

FEATURES

- 15/24 dBm P1dB/PSAT
- 92-96 GHz coverage
- W-band
- 18 dB gain

DESCRIPTION

gAPZ0045 is a power amplifier in the 92-96 GHz frequency band suitable for E/W-band point-to-point communication and 94 GHz automotive radar and imaging. The PA's output stage has four parallel HEMTs to increase output power. The PA has high gain, high linearity, low input/output return loss and flat gain response.

TYPICAL APPLICATIONS

- 94 GHz radar and imaging
- Point-to-point communication
- Instrumentation
- Fiber over radio

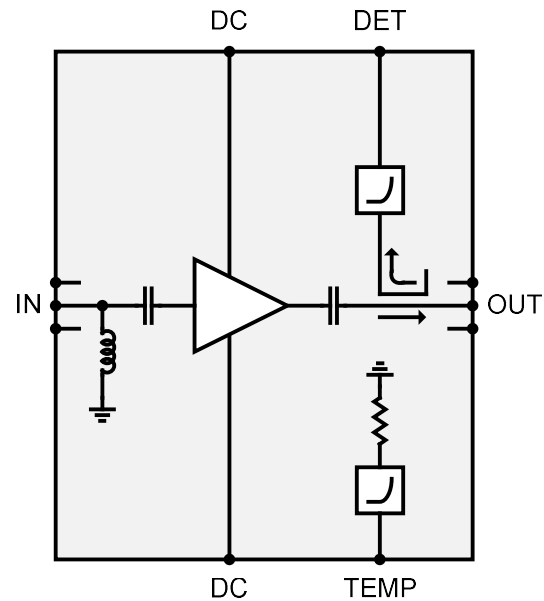


Figure 1. Block diagram of the PA.

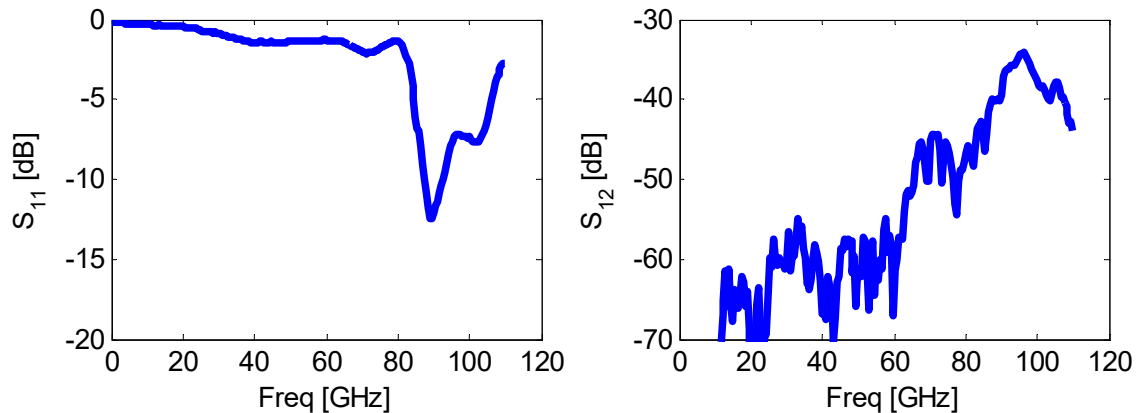
ELECTRICAL PERFORMANCE

Table 1. Electrical performance $T_A=25^\circ\text{C}$

Parameter	Min	Typ	Max	Unit
Frequency	92 (80)		96 (100)	GHz
Gain	16	18	20	dB
P1dB	15	16	17	dBm
PSAT	23	24	25	dBm
PAE			8	%
Input return loss	7			dB
Output return loss	6			dB
NF		8	11	dB
Detector sensitivity		TBD		V/W
Power consumption		2200		mW

MEASURED PERFORMANCE

Measurements have been performed on-wafer with RF input power = -10 dBm/tone, tone separation = 10 MHz, $T_A = 25^\circ\text{C}$ and typical bias settings if not specified differently.



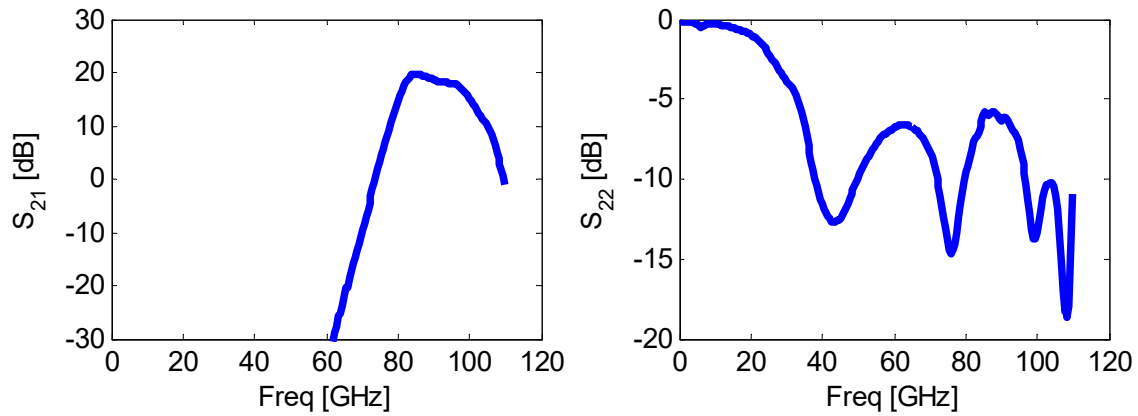


Figure 2. Small signal response from 0-120 GHz at nominal bias. (Upper left): Input matching. (Upper right): Reverse isolation. (Lower left): Small-signal gain. (Lower right): Output matching.

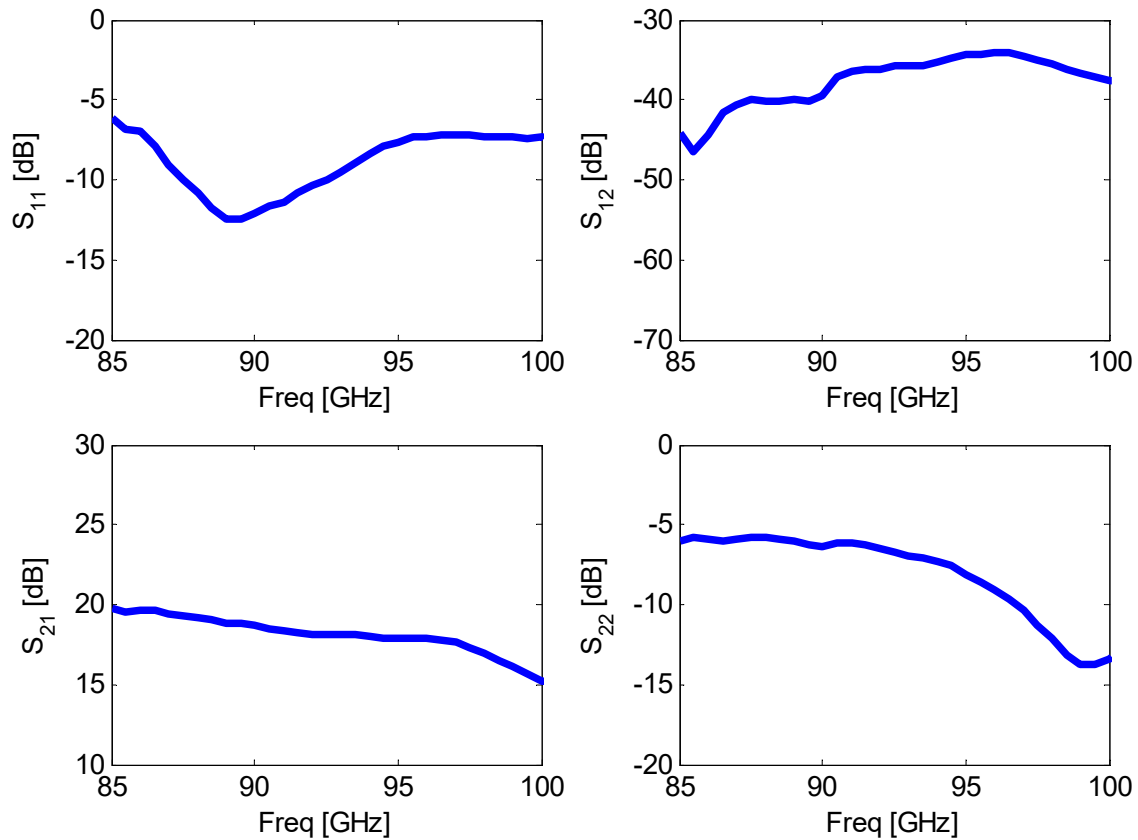


Figure 3. Small signal response within the W-band at nominal bias. (Upper left): Input matching. (Upper right): Reverse isolation. (Lower left): Small-signal gain. (Lower right): Output matching.

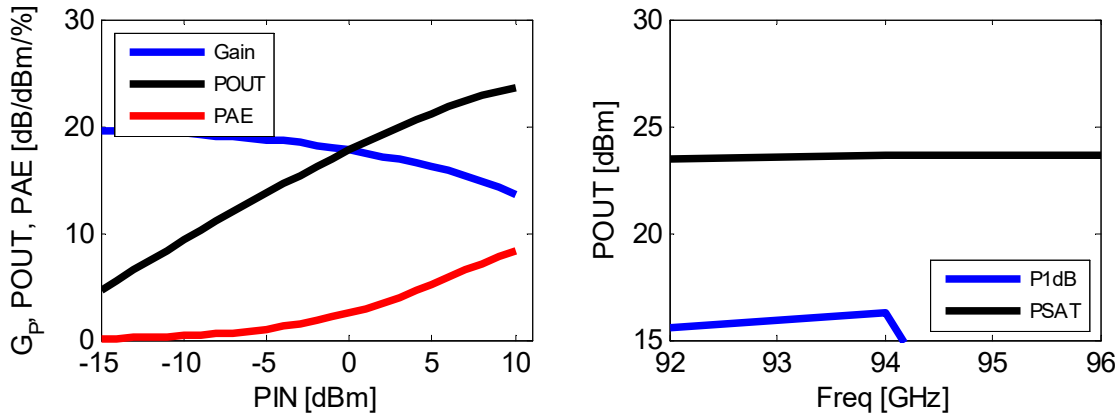


Figure 4. (Left): Output power vs input power at 94 GHz. (Right): P1dB and PSAT versus frequency.

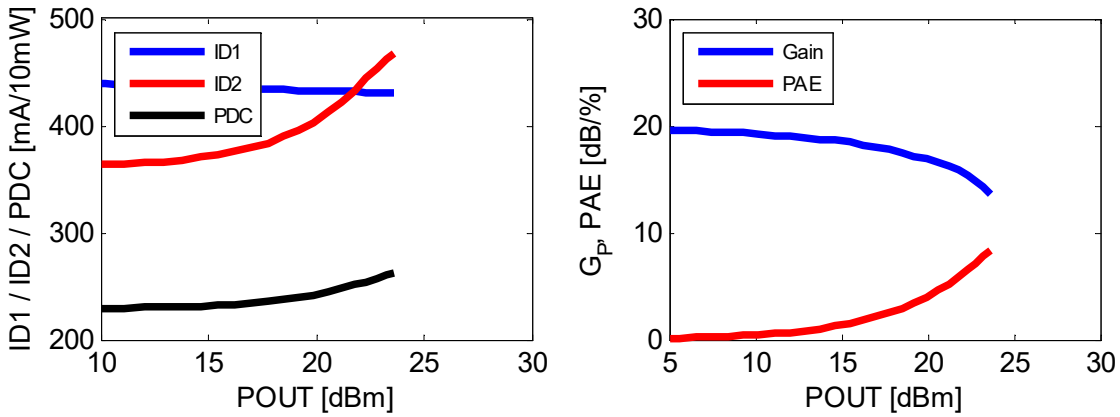


Figure 5. (Left): Power dissipation and drain currents ID1 and ID2 vs output power at 94 GHz. (Right): Efficiency vs output power at 94 GHz.

RECOMMENDED OPERATING CONDITIONS

Bias should first be applied to the gates (VG...) followed by the drains (VD...). The gate voltages must be adjusted within the min/max range indicated in Table 2-5 to obtain the specified drain currents. The drain currents are stated with all input signals off.

Table 2. Electrical settings on connector P1

Connector P1	Pad No.	Bias settings (V / mA)			Function
		Min	Typ	Max	
NC	1				NC
VOUT_DET	2	0		2.0	Output
VREF_DET	3	0	0.2		Output
VG_DET ^[1]	4	-1.0	-0.8	-0.6	Input
VD2 ^[2]	5	3.2	3.3 / 360 ^[3]	3.4	Input
GND	6				Ground
VG2 ^[2]	7	-0.7	-0.5	-0.3	Input
VG1 ^[2]	8	-0.7	-0.5	-0.3	Input
VD1 ^[2]	9	2.4	2.5 / 420 ^[3]	2.6	Input
NC	10				NC
NC	11				NC

Table 3. Electrical settings on connector P2

Connector P2	Pad No.	Settings	Function
GND	1		Ground
RF_OUT	2	Z ₀ = 50 Ohm, AC coupled	Output
GND	3		Ground

^[1] Maximum sensitivity is achieved at threshold voltage. Lower VG_DET until the current reaches 0 mA on VD_DET.

^[2] VG1, VG2, VD1 and VD2 are physically connected across the chip via P1 and P3. Both connectors must be biased for maximum performance.

^[3] Total current for connectors P1 and P3.

Table 4. Electrical settings on connector P3

Connector P3	Pad No.	Bias settings (V / mA)			Function
		Min	Typ	Max	
NC	1				NC
NC	2				NC
VD1 ^[2]	3	2.4	2.5 / 420 ^[3]	2.6	Input
VG1 ^[2]	4	-0.7	-0.5	-0.2	Input
VG2 ^[2]	5	-0.7	-0.5	-0.2	Input
GND	6				Ground
VD2 ^[2]	7	3.2	3.3 / 360 ^[3]	3.4	Input
VG_TEMP	8				Input
NC	9				NC
NC	10				NC
NC	11				NC

Table 5. Electrical settings on connector P4

Connector P4	Pad No.	Settings	Function
GND	1		Ground
RF_IN	2	$Z_0 = 50 \text{ Ohm}$, AC coupled	Input
GND	3		Ground

Table 6. Absolute maximum ratings

Gate-source voltage	-2 to +0.7 V
Drain-source voltage	4.5 V
Gate-drain breakdown voltage	8 V
Drain current (ID1, ID2)	720 mA
RF input power	+20 dBm
Operating temperature	-40 to + 85°C
Storage temperature	-65 to +150°C

OUTLINE DRAWING

Mechanical drawing with pad locations is also available in dxf-file format on the web. Substrate thickness is 50 μm (GaAs).

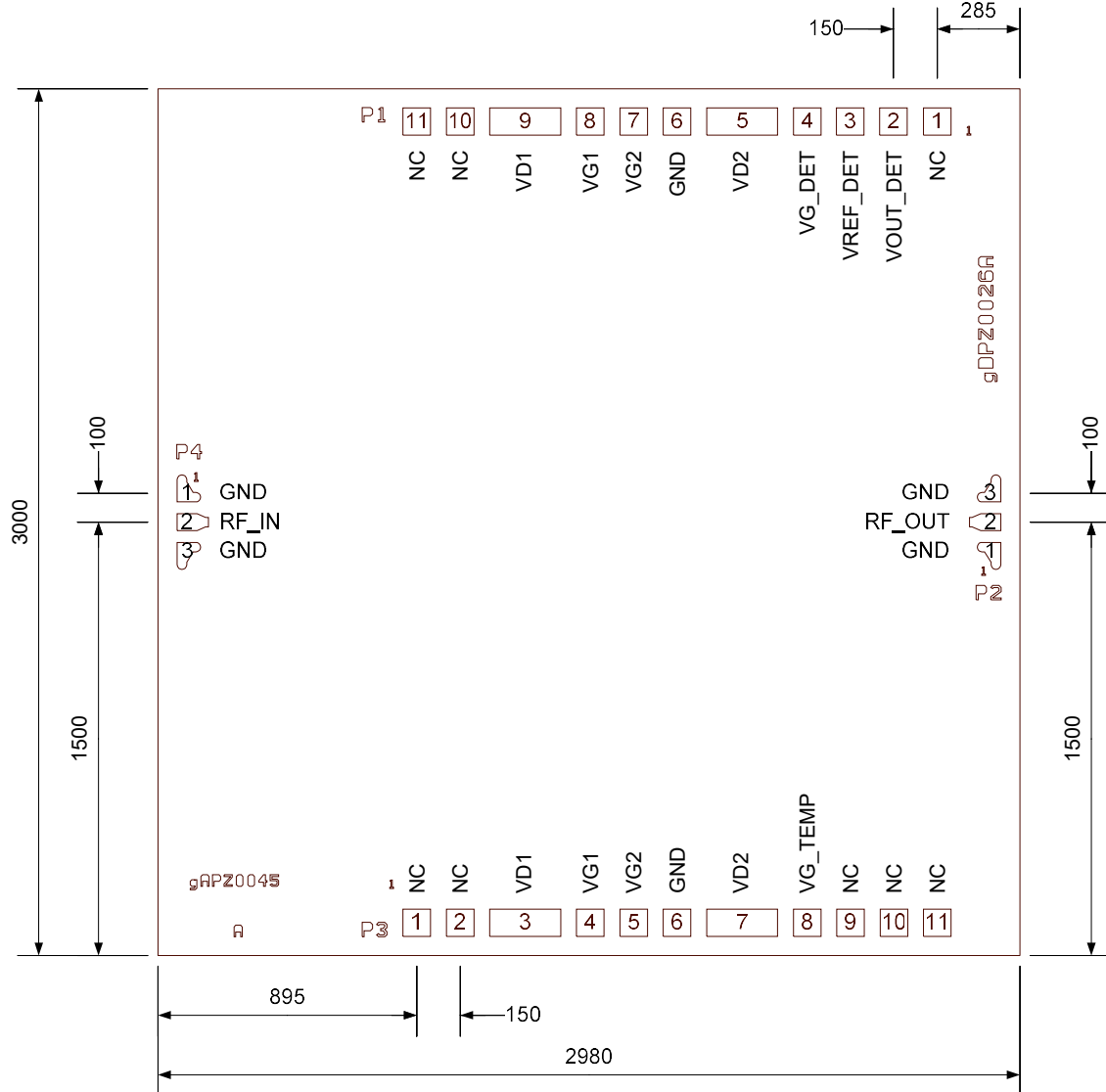


Figure 6. Outline drawing of the MMIC. Dimensions are in μm .