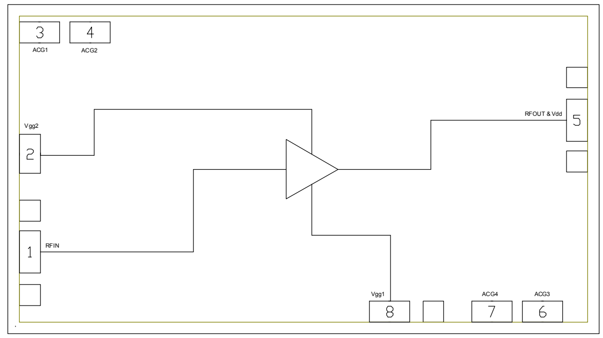
CMD292

DC-30 GHz Distributed Driver Amplifier

Features

- ► Ultra wideband performance
- ► High linearity
- ► High output power
- ► HMC994 replacement
- ► Small die size

Functional Block Diagram



Description

The CMD292 is wideband GaAs MMIC distributed driver amplifier die which operates from DC to 30 GHz. The amplifier delivers 13 dB of gain with a corresponding output 1 dB compression point of +27 dBm and output IP3 of 33 dBm at 15 GHz. The CMD292 is a 50 ohm matched design which eliminates the need for RF port matching. The CMD292 offers full passivation for increased reliability and moisture protection.

Electrical Performance – V_{dd} = 10.0 V, V_{gg2} = 3.5 V, I_{dd} = 250 mA, T_A = 25 °C, F = 15 GHz

Parameter	Min	Typ	Max	Units
Frequency Range		DC – 30		GHz
Gain		13		dB
Noise Figure		3		dB
Input Return Loss		20		dB
Output Return Loss		23		dB
Output P1dB		27		dBm
Output Psat		28.5		dBm
Output IP3		33		dBm
Supply Current		250		mA

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Specifications

Absolute Maximum Ratings

Parameter	Rating
Drain Voltage, Vdd	11.2 V
Gate1 Voltage, Vgg1	-2.5 V to 0 V
Gate2 Voltage, Vgg2	5.5 V
RF Input Power	+28 dBm
Channel Temperature, Tch	150 °C
Power Dissipation, Pdiss	3.778 W
Thermal Resistance, Θ_{JC}	17.2 °C/W
Operating Temperature	-55 to 85 °C
Storage Temperature	-55 to 150 °C

Exceeding any one or combination of the maximum ratings may cause permanent damage to the device.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Vdd	8.0	10.0	11.0	V
Idd		250		mA
Vgg1		-0.5		V
Vgg2		3.5		V

Electrical performance is measured at specific test conditions. Electrical specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications – V_{dd} = 10.0 V, V_{gg2} = 3.5 V, I_{dd} = 250 mA T_A = 25 °C

Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Frequency Range	DC - 10			10 - 20			20 - 30			GHz
Gain	9.5	12.5		10	13		11	14.5		dB
Noise Figure		4			3			4		dB
Input Return Loss		23			20			17		dB
Output Return Loss		20			23			15		dB
Output P1dB	24.5	27.5		24.5	27.5		22	26		dBm
Output IP3		37			33			30		dBm
Supply Current		250	300		250	300		250	300	mA
Gain Temperature Coefficient		0.013			0.015			0.019		dB/°C
Noise Figure Temp. Coefficient		0.01			0.012			0.017		dB/°C

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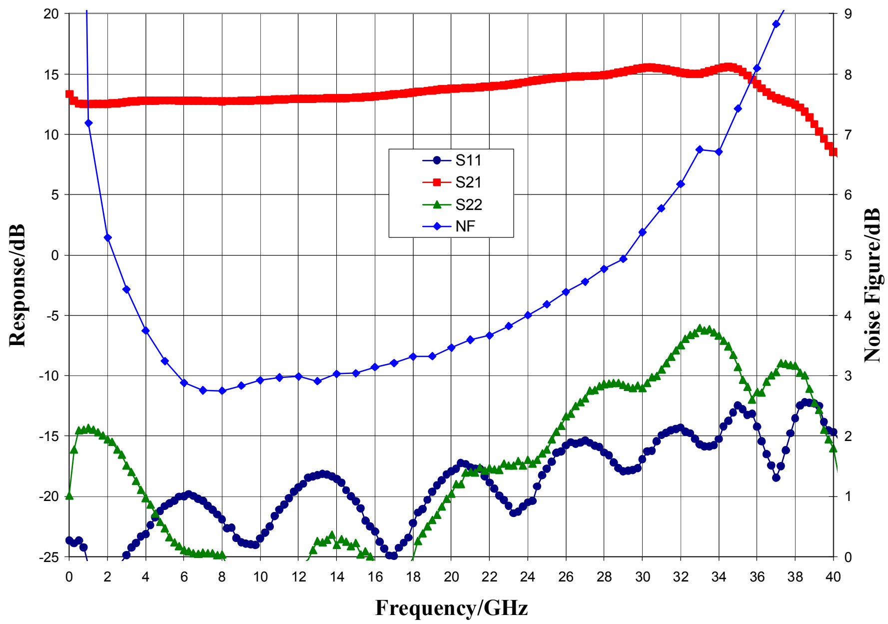
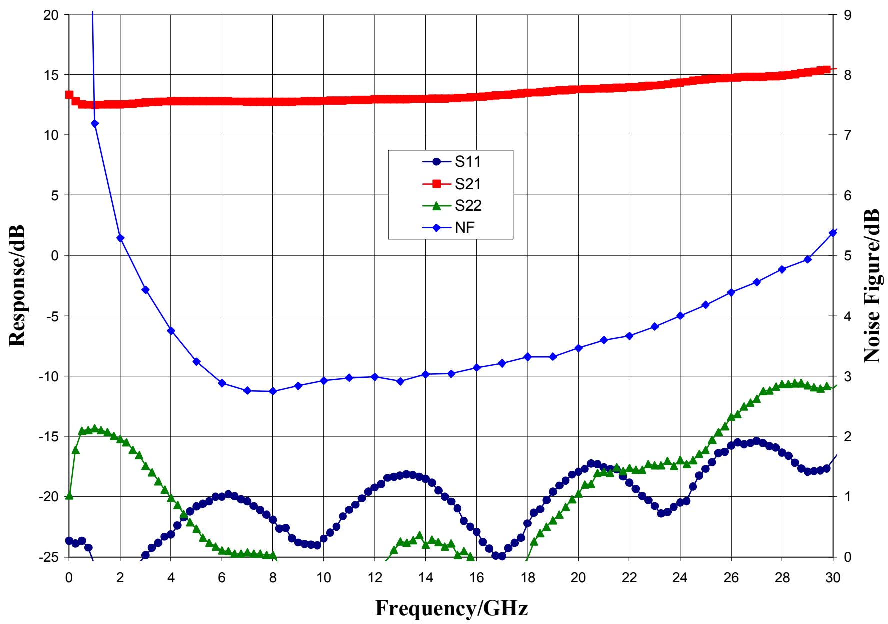
Typical Performance

Broadband Performance, V_{dd} = 10 V, V_{gg2} = 3.5 V, I_{dd} = 250 mA, T_A = 25 °C



Narrow-band Performance, V_{dd} = 10 V, V_{gg2} = 3.5 V, I_{dd} = 250 mA, T_A = 25 °C



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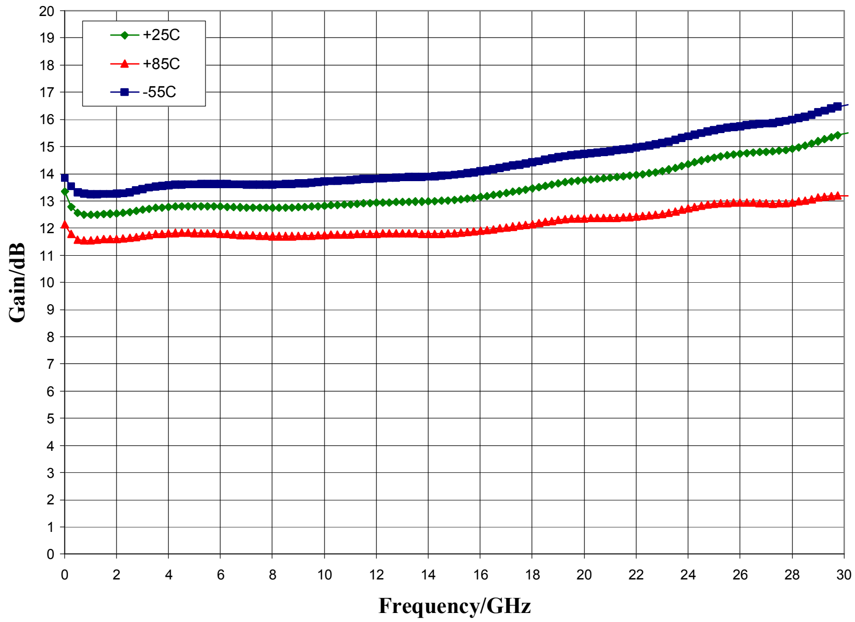
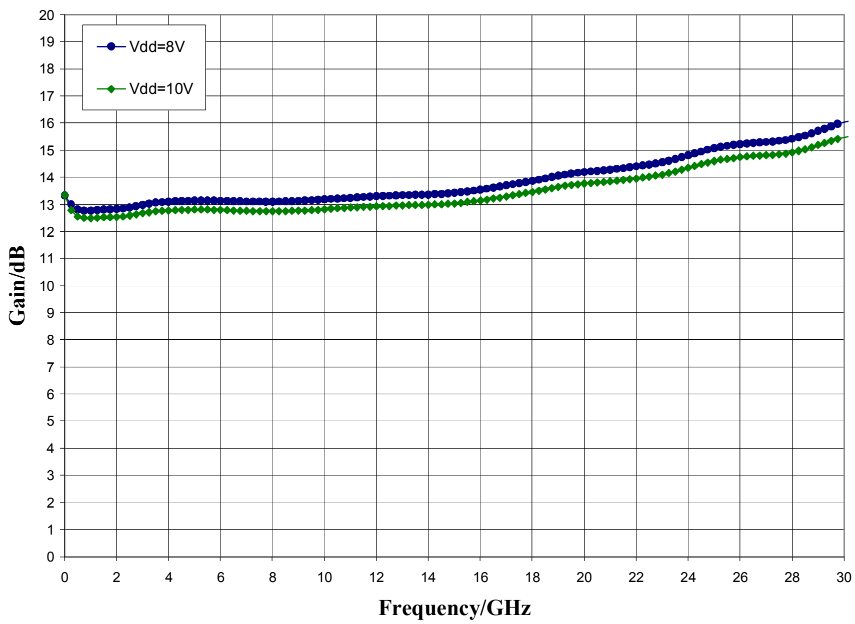
Typical Performance

Gain vs. Temperature, V_{dd} = 10 V, V_{gg2} = 3.5 V



Gain vs. Vdd, V_{gg2} = 3.5 V, I_{dd} = 250 mA, T_A = 25 °C



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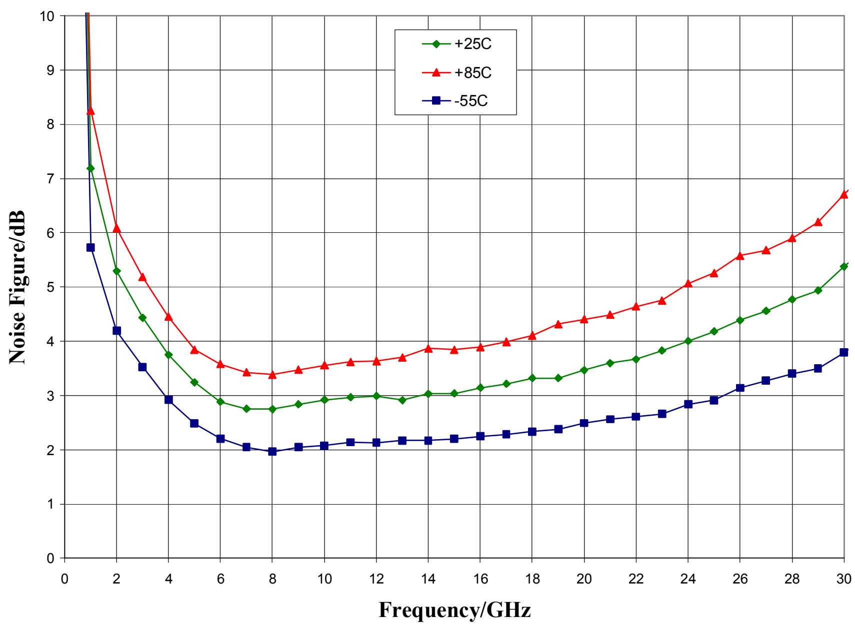
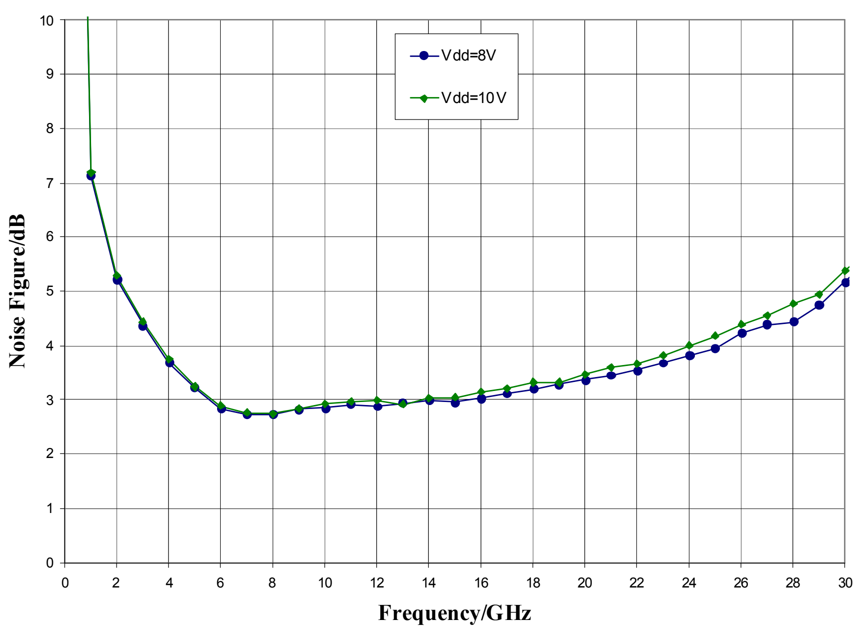
Typical Performance

Noise Figure vs. Temperature, V_{dd} = 10 V, V_{gg2} = 3.5 V



Noise Figure vs. Vdd, V_{gg2} = 3.5 V, I_{dd} = 250 mA, T_A = 25 °C



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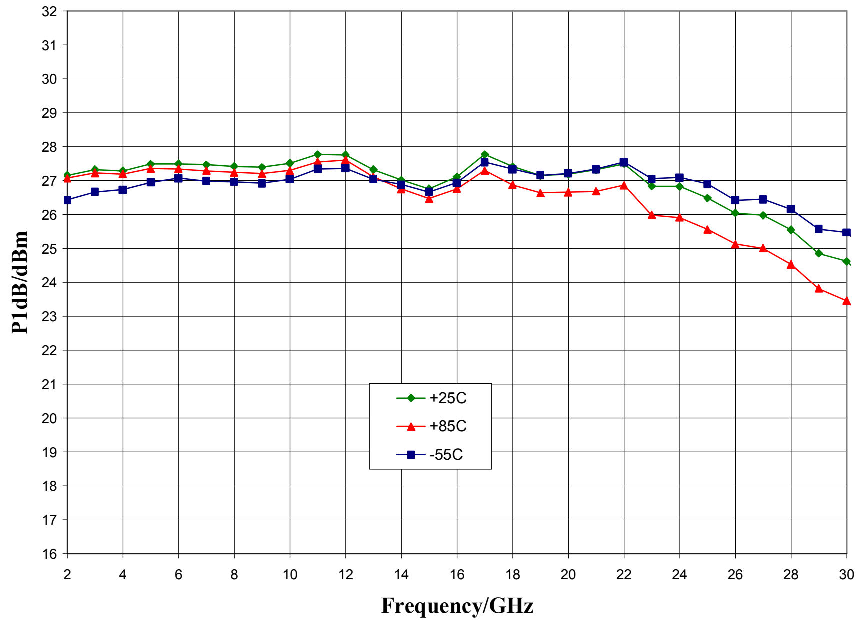
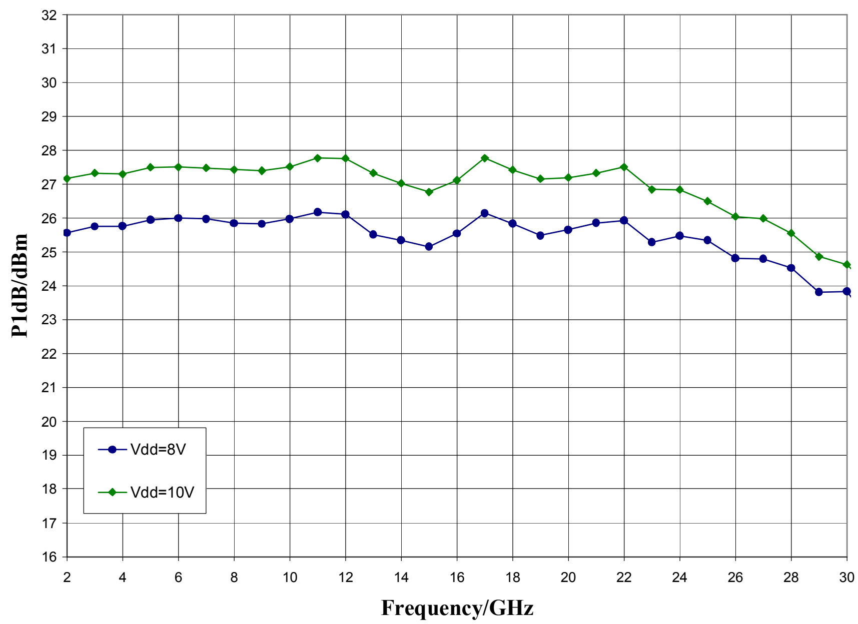
Typical Performance

P1dB vs. Temperature, V_{dd} = 10 V, V_{gg2} = 3.5 V



P1dB vs. Vdd, V_{gg2} = 3.5 V, I_{dd} = 250 mA, T_A = 25 °C



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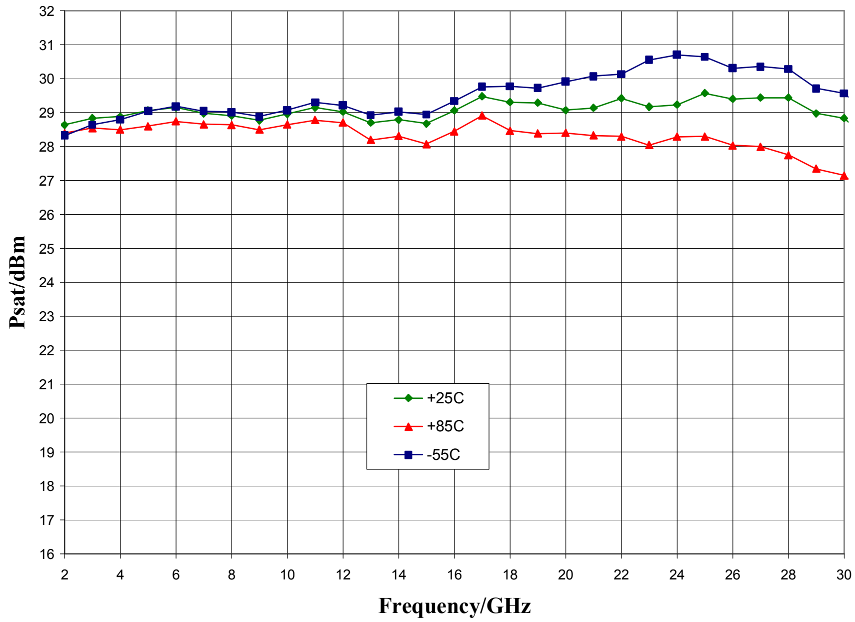
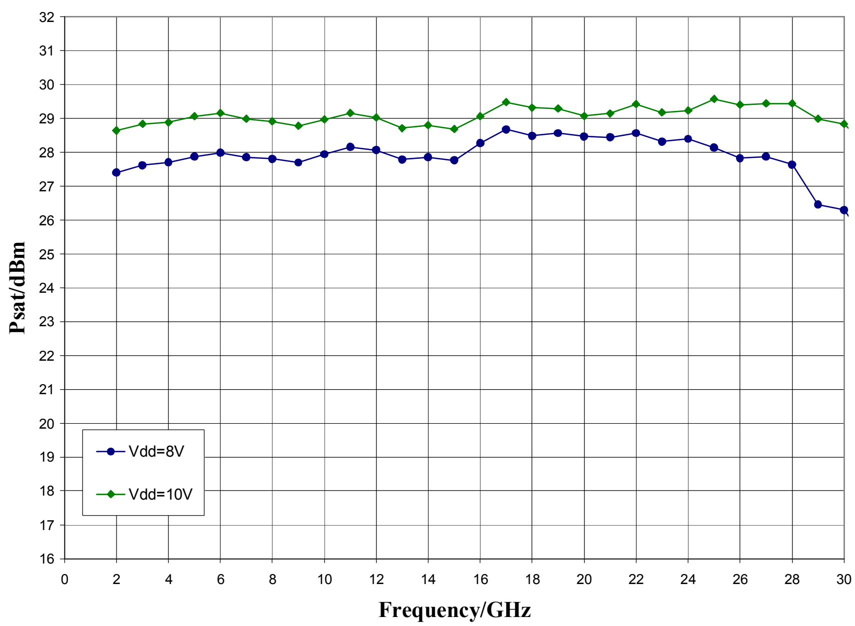
Typical Performance

Psat vs. Temperature, V_{dd} = 10 V, V_{gg2} = 3.5 V



Psat vs. Vdd, V_{gg2} = 3.5 V, I_{dd} = 250 mA, T_A = 25 ^oC



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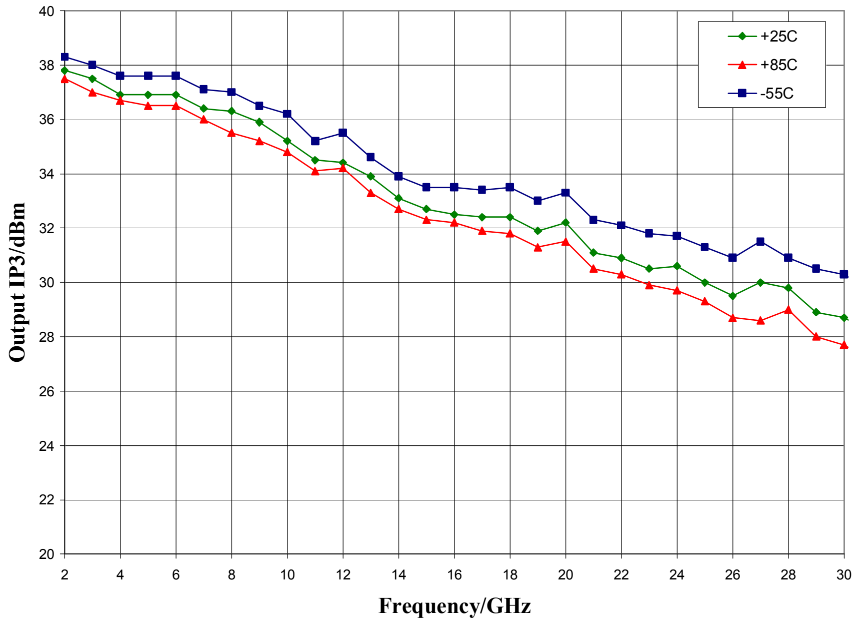
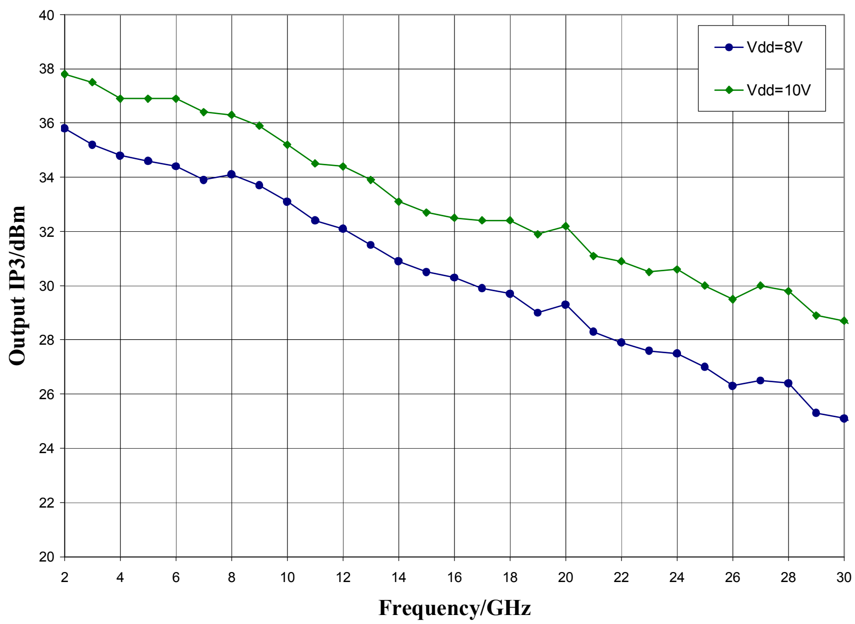
Typical Performance

Output IP3 vs. Temperature, V_{dd} = 10 V, V_{gg2} = 3.5 V



Output IP3 vs. Vdd, V_{gg2} = 3.5 V, I_{dd} = 250 mA, T_A = 25 °C



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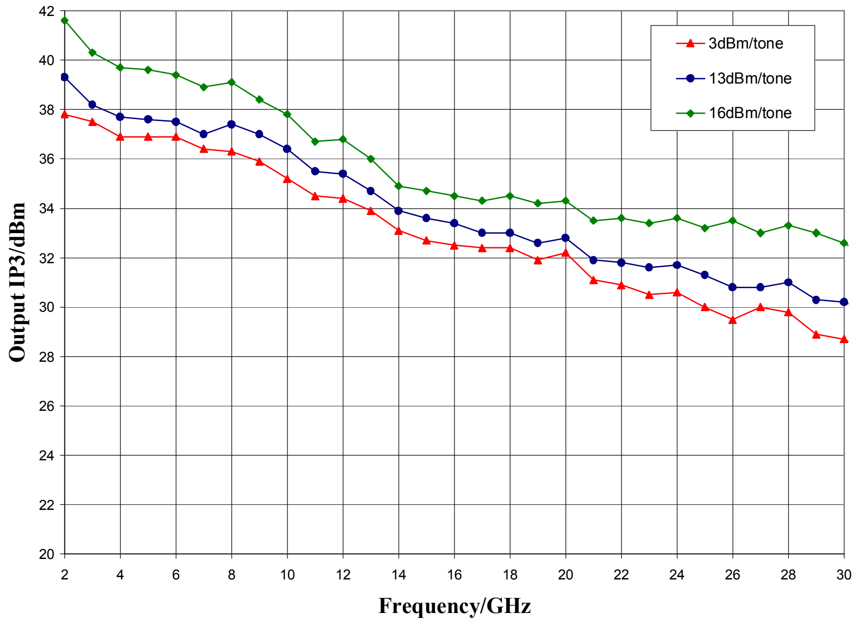
Typical Performance

Output IP3 vs. Output Power, V_{dd} = 10V, V_{gg2} = 3.5 V, I_{dd} = 250 mA, T_A = 25 °C



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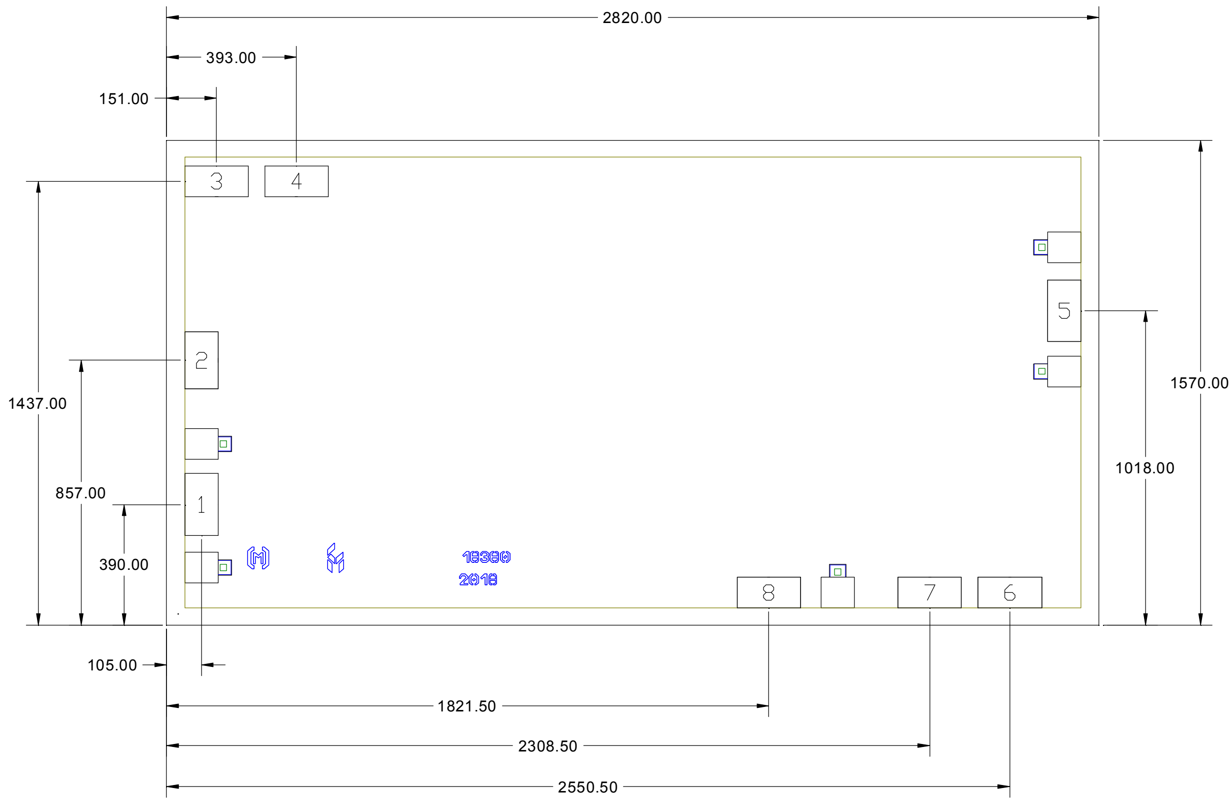
Mechanical Information

Die Outline (all dimensions in microns)



Notes:
1. No connection required for unlabeled pads
2. Backside is RF and DC ground
3. Backside and bond pad metal: Gold
4. Die is 70 microns thick
5. DC bond pads (2, 3, 4, 6, 7, and 8) are 100 x 192 microns
6. RF bond pads (1 and 5) are 100 x 200 microns

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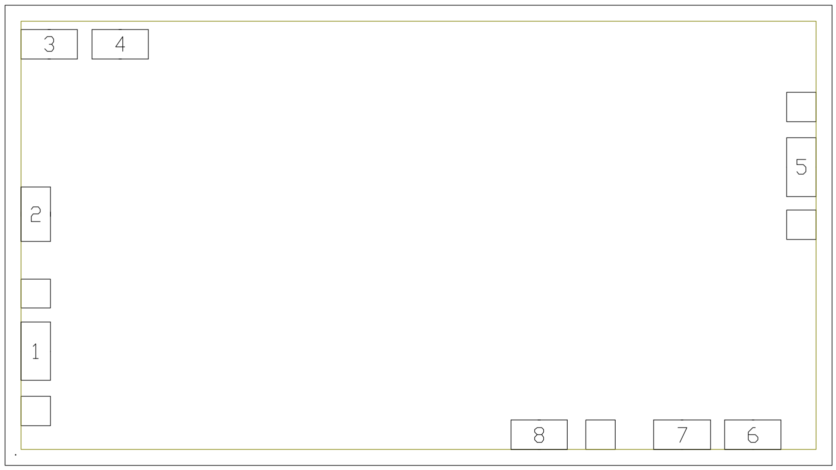
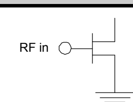
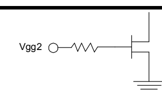
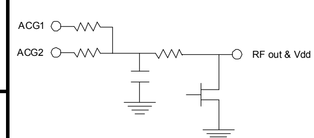
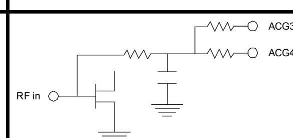
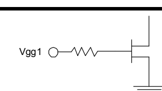
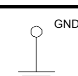
Pad Description

Pad Diagram



Functional Description

Pad	Function	Description	Schematic
1	RF in	50 ohm matched input	
2	Vgg2	Power supply voltage Decoupling and bypass caps required	
3, 4	ACG1, 2	Low frequency termination. Attach bypass capacitor per application circuit	
5	RF out & Vdd	Power supply voltage and 50 ohm matched output	
6, 7	ACG3, 4	Low frequency termination. Attach bypass capacitor per application circuit	
8	Vgg1	Power supply voltage Decoupling and bypass caps required	
Backside	Ground	Connect to RF / DC ground	

Applications Information

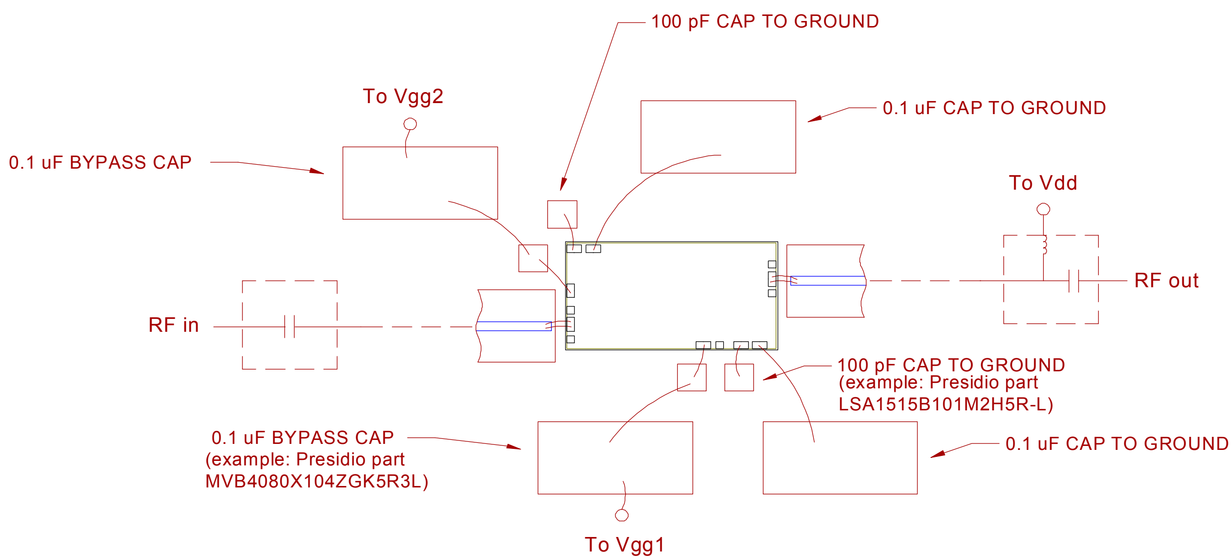
Assembly Guidelines

The backside of the CMD292 is RF ground. Die attach should be accomplished with electrically and thermally conductive epoxy only. Eutectic attach is not recommended. Standard assembly procedures should be followed for high frequency devices. The top surface of the semiconductor should be made planar to the adjacent RF transmission lines, and the RF decoupling capacitors placed in close proximity to the DC connections on chip.

RF connections should be made as short as possible to reduce the inductive effect of the bond wire. Use of a 0.8 mil thermosonic wedge bonding is highly recommended as the loop height will be minimized. The RF input and output require a double bond wire as shown.

The semiconductor is 70 um thick and should be handled by the sides of the die or with a custom collect. Do not make contact directly with the die surface as this will damage the monolithic circuitry. Handle with care.

Assembly Diagram



GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

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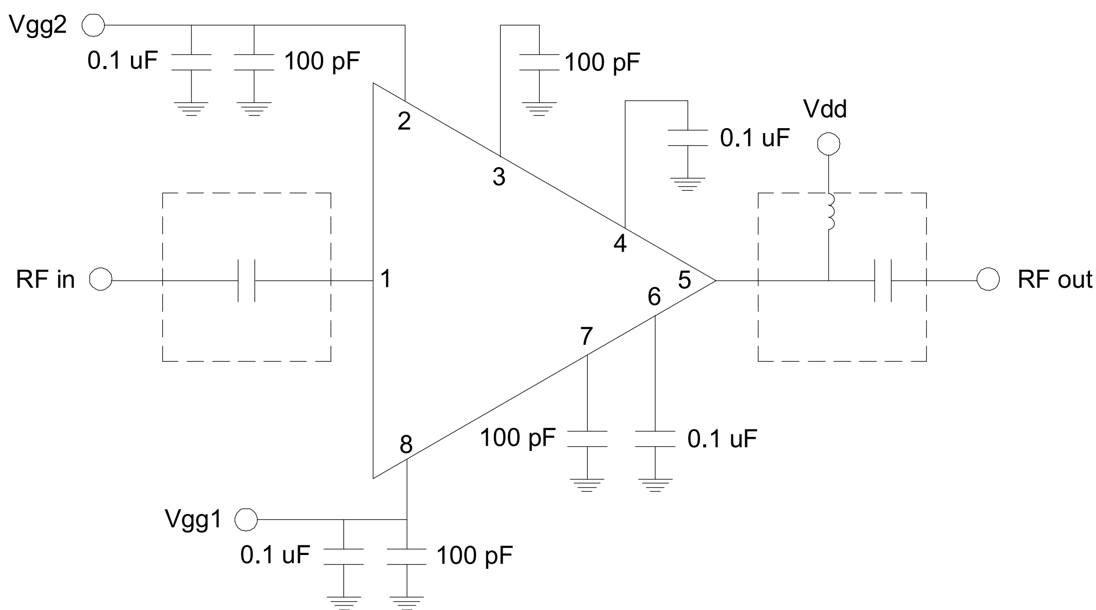
Applications Information

Application Circuit



Note: Drain voltage (Vdd) must be applied through a broadband bias tee or external bias network. External DC block is required on RF input.

Biasing and Operation

The CMD292 is biased with a positive drain supply and a positive and negative gate supply. Performance is optimized when the drain voltage (V_{dd}) is set to +10 V and gate2 voltage (V_{gg2}) is set to +3.5 V. The nominal gate1 voltage (V_{gg1}) is -0.5 V.

Turn ON procedure:

1.Apply gate1 voltage V_{gg1} and set to -2 V
2.Apply gate2 voltage V_{gg2} and set to +3.5 V
3.Apply drain voltage V_{dd} and set to +10 V
4.Increase V_{gg1} (less negative) to achieve a drain current of 250 mA

Turn OFF procedure:

1.Turn off drain voltage V_{dd}
2.Turn off gate2 voltage V_{gg2}
3.Turn off gate1 voltage V_{gg1}

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