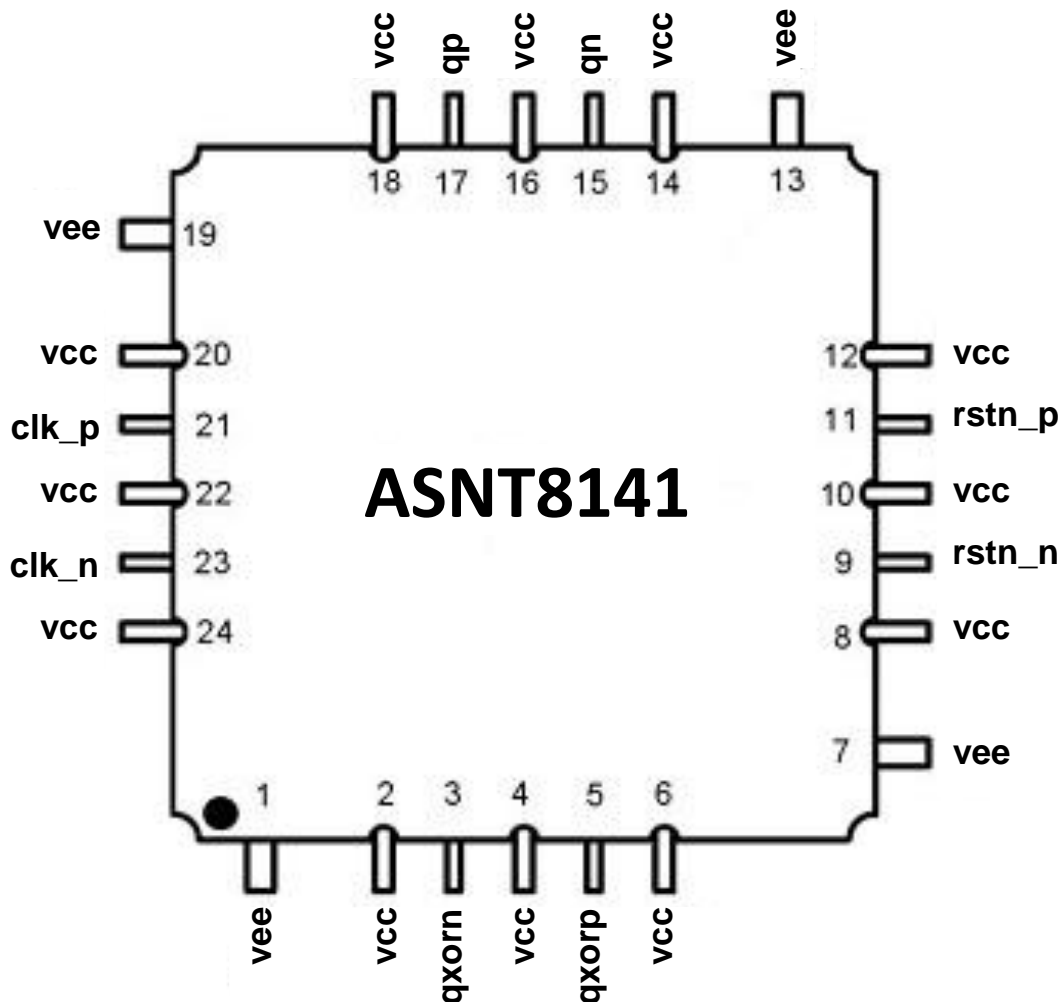




ASNT8141-KMC

DC-23Gbps PRBS Generator with the $(x^7 + x^6 + 1)$ Polynomial

- Full-length (2^7-1) pseudo-random binary sequence (PRBS) generator
- DC to 23Gbps output data rate
- Additional output delayed by half of the sequence period
- Asynchronous reset signal for elimination of the “all zeros” initial state
- Fully differential CML input interface
- Fully differential CML output interface with 400mV single-ended swing
- Single +3.3V or -3.3V power supply
- Power consumption: 530mW
- Custom CQFP 24-pin package



DESCRIPTION

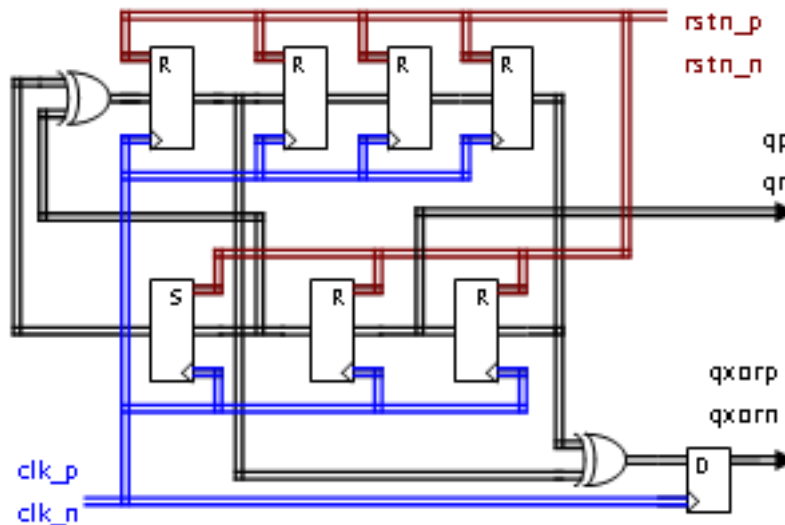


Fig. 1. Functional Block Diagram

The ASNT8141-KMC SiGe IC shown in Fig. 1 provides a full 127-bit long pseudo-random binary sequence (PRBS) signal according to the polynomial $(x^7 + x^6 + 1)$, where x^D represents a delay of D clock cycles. This is implemented as a linear feedback shift register (LFSR) in which the outputs of the seventh and sixth flip-flops are combined together by an XOR function and provided as an input to the first flip-flop of the register.

The LFSR-based PRBS generator produces 127 binary states, excluding the “all zeros” state that is illegal for the XOR-based configuration. To eliminate this state that locks the LFSR and prevents PRBS generation, an asynchronous external active-low preset signal *rstn_p/rstn_n* is implemented in the circuit. When the preset is asserted, LFSR is set to the “1000000” state containing one logic “1” value that is enough for the activation of the PRBS generation. When the preset is released, the chip delivers one consecutive bit of the PRBS signal to output pins *qp/qn* per each rising edge of clock *clk_p/clk_n*, starting from the above mentioned state.

An additional copy of the same PRBS signal delayed by 63 bits (half of the sequence period) is delivered to pins *qxorp/qxorn* and can be used to double the frequency of the output signal using an external multiplexer (e.g. ASNT5150 part) as shown in Fig. 2.

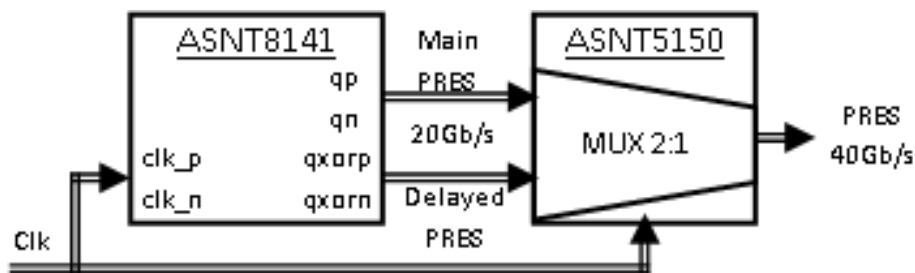


Fig. 2. PRBS Frequency Doubling



The simulated eyes for both signals are shown in Fig. 3.

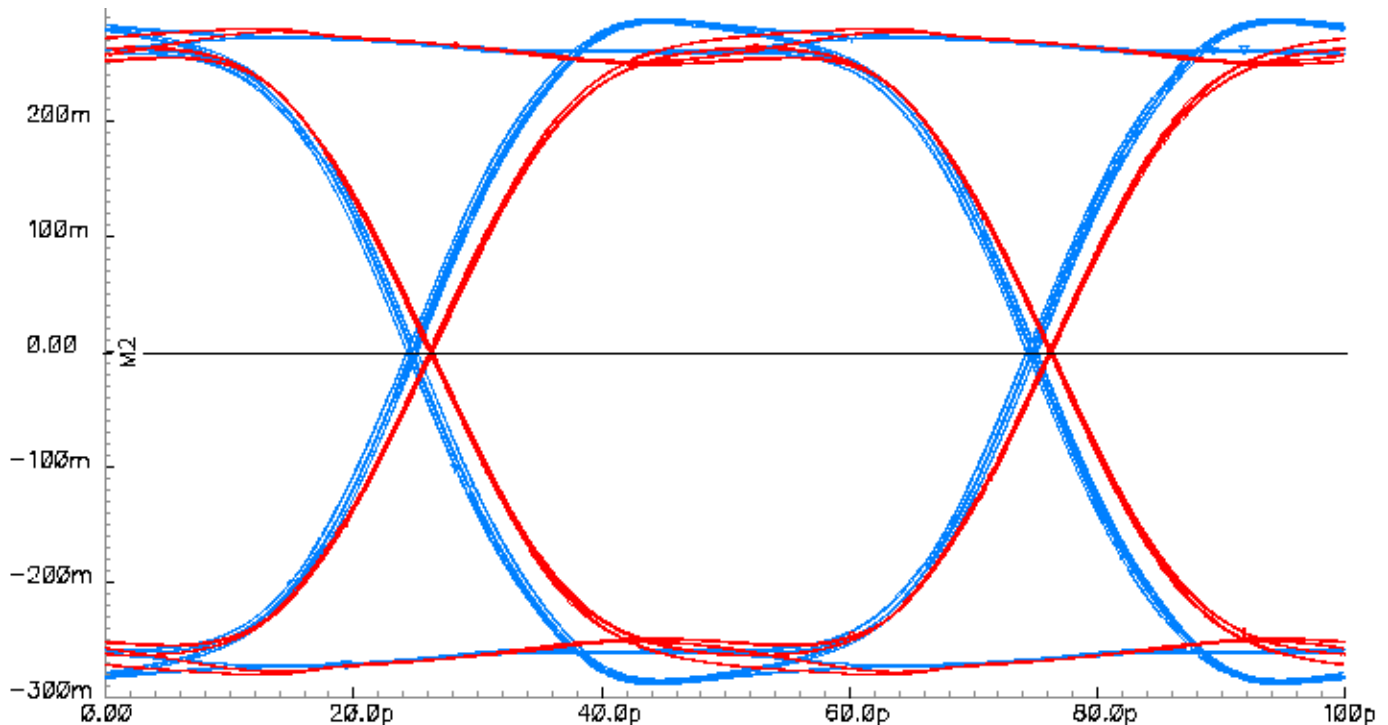


Fig. 3. 20Gbps PRBS Output Eye Diagram (Simulation, Slow Corner, 125°C)

All I/O stages are back terminated to v_{CC} with on-chip 50Ω resistors and may be used in either DC or AC coupling modes (see also POWER SUPPLY CONFIGURATION). In the first mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the second mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply ($v_{CC} = 0.0V = \text{ground}$ and $v_{EE} = -3.3V$), or a positive supply ($v_{CC} = +3.3V$ and $v_{EE} = 0.0V = \text{ground}$). In case of a positive supply, all I/Os need AC termination when connected to any devices with 50Ω termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume $v_{CC} = 0.0V$ and $v_{EE} = -3.3V$.



ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	V
Power Consumption		0.58	W
RF Input Voltage Swing (SE)		1.0	V
Case Temperature		+90	°C
Storage Temperature	-40	+100	°C
Operational Humidity	10	98	%
Storage Humidity	10	98	%

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	No.	Type	
High-Speed I/Os			
rstn_p	11	CML input	Differential high-speed asynchronous reset (active low) inputs with internal SE 50Ohm termination to vcc
rstn_n	9		
clk_p	21	CML input	Differential high-speed clock input signals with internal 50Ohm termination to vcc
clk_n	23		
qp	17	CML output	Differential high-speed data outputs. Require external SE 50Ohm termination to vcc
qn	15		
qxorp	5	CML output	Differential delayed sequence high-speed data outputs. Require external SE 50Ohm termination to vcc
qxorn	3		
Supply and Termination Voltages			
Name	Description	Pin Number	
vcc	Positive power supply (+3.3V or 0)	2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24	
vee	Negative power supply (0V or -3.3V)	1, 7, 13, 19	



ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	V	±6%
vcc		0.0		V	External ground
I _{vee}		160		mA	
Power consumption		530		mW	
Junction temperature	-40	25	125	°C	
HS Input Clock (clk_p/clk_n)					
Frequency	DC		23	GHz	
Swing	0.05		0.8	V	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	V	Must match for both inputs
HS Output Data (qp/qn, qxorp/qxorn)					
Swing (SE)	280	440		mV	
CM Voltage Level	vcc-0.8		vcc	V	
Output Jitter		2.5		ps	Peak-to-peak
Reset Signal (rstn_p/rstn_n)					
Frequency	DC		15	GHz	
Rise time			20	%	of the clock period
Recovery time	36			ps	
Swing	0.05		0.8	V	Differential p-p
CM Voltage Level	vcc-0.8		vcc	V	

PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFP package shown in Fig. 4. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT8141-KMC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

The IC complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all 6 substances.

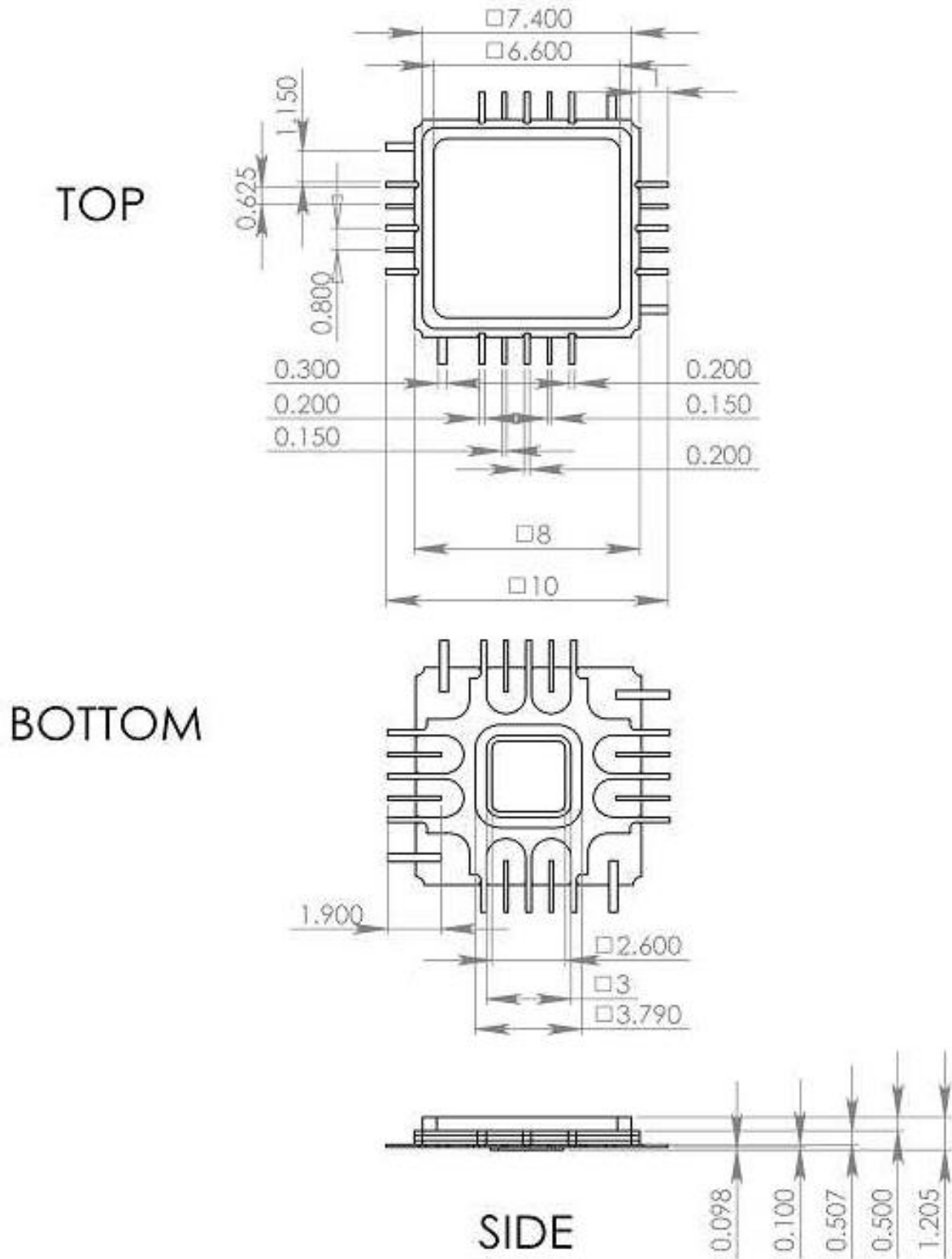


Fig. 4. CQFP 24-Pin Package Drawing (All Dimensions in mm)



REVISION HISTORY

Revision	Date	Changes
1.6.1	11-2015	Updated description Updated power supply configuration Updated absolute maximum ratings section Corrected electrical characteristics table Updated package information section
1.3.1	08-2013	Corrected description
1.2.1	02-2013	Corrected title Corrected description Corrected terminal functions table Updated electrical characteristics table Revised package information section
1.1.1	01-2013	Updated power and current consumption
1.0.1	01-2013	First release