ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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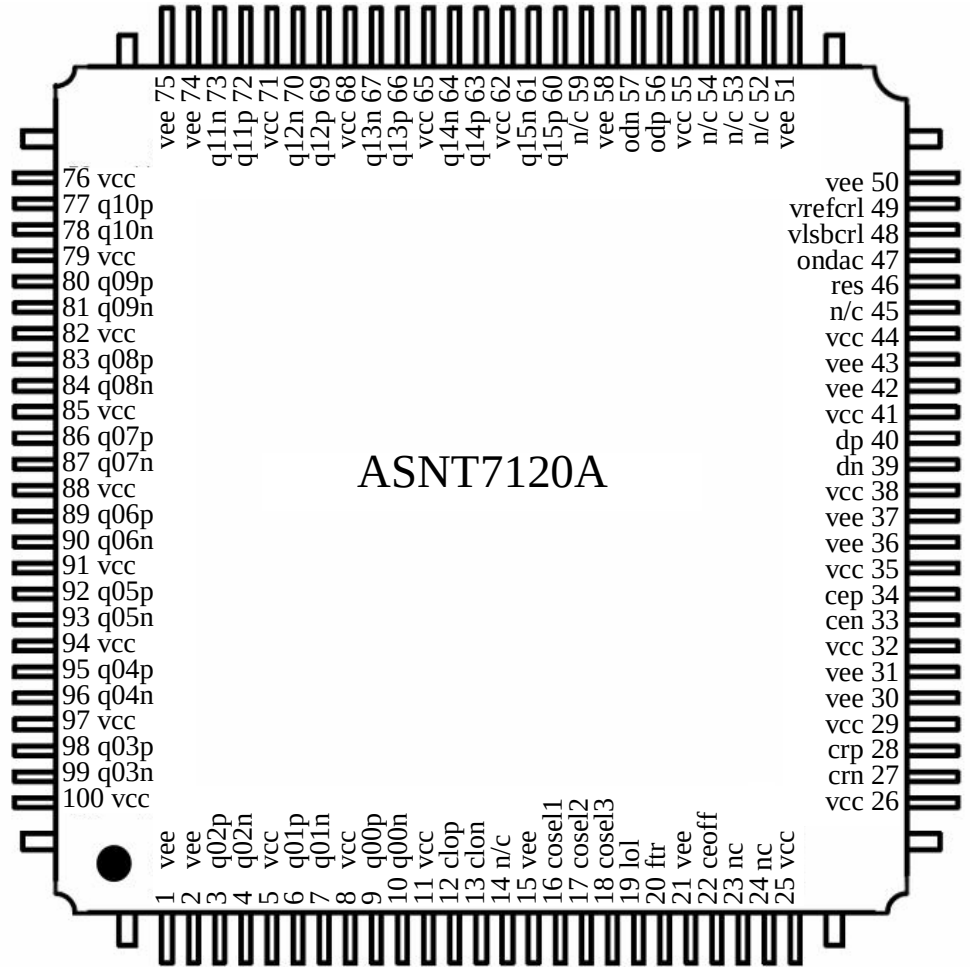
ASNT7120A-KMA
15*GS/s*, 4-bit Flash Analog-to-Digital Converter

- 20*GHz* analog input bandwidth
- Selectable clocking mode: external high-speed clock or internal PLL with external reference clock
- Broadband operation in external clocking mode: DC-15*GS/s*
- On-chip PLL with a central frequency of 10*GHz*
- Optional external preset of the internal clock divider
- Internal demultiplexer 4-to-16 for the output data rate reduction
- Differential CML input clock buffer and linear input data buffer
- Proprietary low-power LVDS output interface
- Selectable output clock frequency and polarity
- Selectable on-chip digital-to-analog converter for self-testing
- Single +3.5*V* power supply
- Power consumption: 3.6*W*
- Custom 100-pin metal-ceramic package



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DESCRIPTION

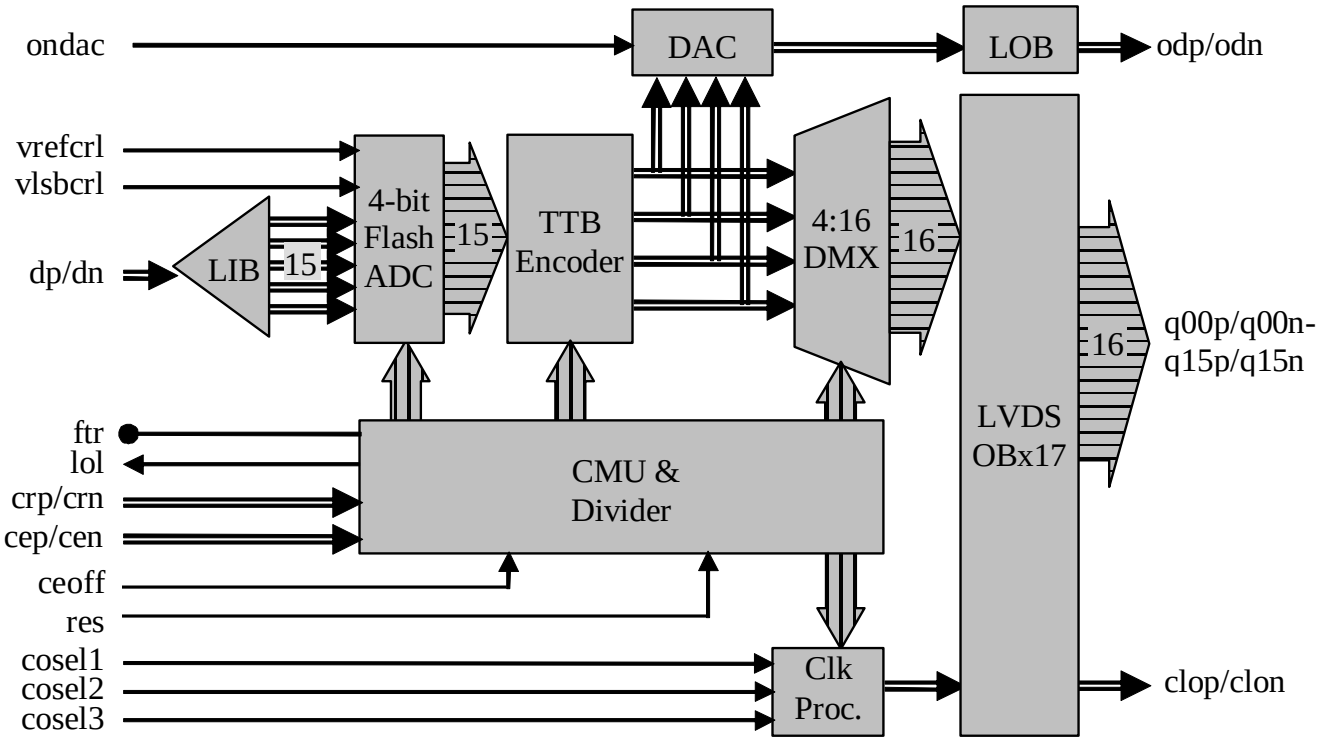

Fig. 1. Functional Block Diagram

The ASNT7120A-KMA is a 4-bit flash analog to digital converter (ADC) featuring a high sampling rate and wide analog front-end bandwidth. The ADC system shown in Fig. 1 includes a linear input buffer (LIB) with tree-type architecture and a CML-type input interface with internal 50*Ohm* single-ended terminations to vcc. The buffer delivers 15 matching copies of the input analog data signal dp/dn to the 4-bit flash ADC. The ADC creates 15 samples of the input data in thermometer code, which are then converted by a thermometer-to-binary encoder (TTB Encoder) into 4-bit binary words with a data rate *f*. The ADC thresholds are controlled by signals vrefcrl and vlsbcrl. The encoded data is demultiplexed into 16-bit wide words with a data rate *f*/4 and sent to the output through 16 low-power LVDS buffers as signals q00p/q00n-q15p/q15n. An optional digital-to-analog converter (DAC) with an output signal odp/odn can be used to control the ADC's operation. It is enabled by using control signal ondac.

All operations are synchronized by the internal clock multiplication unit (CMU) based on a PLL (phase-locked loop) with an integrated divider and an external loop filter connected to pin ftr. The block can operate in two different modes which are controlled by signal ceoff: clock multiplication (PLL is on, a reference clock is applied to pins crp/crn), and clock division (PLL is off, an external high-speed clock is applied to pins cep/cen). In both modes, the divider generates internal clock signals divided by 2, 4, 8, and 16. The generated divided clocks are sent to different internal blocks. In the CMU's second operational mode, the divider can be preset by external signal res to allow synchronization of parallel-connected ADCs. A PLL lock control output lol is also provided.

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The part operates from a single +3.5*V* power supply. All external control signals are compatible with the 2.5*V* CMOS interface.

Linear Input Buffer (LIB)

The system includes a linear input buffer (LIB) with a tree-type architecture that delivers 15 matching copies of the wide-band input differential analog data signal dp/dn to the 4-bit flash section. Symmetry is closely followed in both schematic and layout to ensure minimal aperture jitter.

Clock Multiplication Unit (CMU) & Divider

The PLL-based CMU with external loop filter connected to pin ftr, as shown in Fig. 2, can operate in two different modes. In the first "clock multiplication" mode (ceoff="1" , default), the CMU multiplies an external reference clock crp/crn with a speed of *f*/16 by means of a PLL with central frequency of *f* and a wide tuning range of the internal VCO (voltage-controlled oscillator). The generated clock is processed by the divider in order to generate internal clock signals divided by 2, 4, 8, and 16.

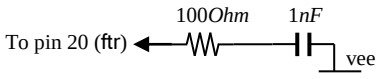

Fig. 2. Recommended External Loop Filter Schematic

In the second "clock division" mode (ceoff="0"), the PLL is disabled and the internal clocks are generated from the external high-speed clock input cep/cen. To align multiple ADCs in parallel, the divider should be preset by the active-high CMOS control signal res.

HS External Clock Input Buffer

The high-speed external clock input buffer can accept high-speed clock signals at its differential CML input port cep/cen. It can also accept a single-ended signal with AC or DC termination. In case of AC termination, the unused pin should be also AC terminated with a 50*Ohm* load. In case of DC termination, a threshold voltage must be applied to the unused pin. The buffer can handle a wide range of input signal amplitudes. The buffer utilizes on-chip single-ended termination of 50*Ohm* to vcc for each input line.

LS Reference Clock Input Buffer

The low-speed reference clock input buffer is a proprietary LVDS buffer with internal 100*Ohm* differential termination between its inputs crp/crn. The buffer exceeds the requirements of standards IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995. It is designed to accept differential signals with amplitudes above 100*mV* peak-to-peak (p-p), a wide range of DC common mode voltages, and AC common mode noise with a frequency up to 5*MHz* and voltage levels ranging from 0 to 2.4*V*.

4-bit Flash Analog to Digital Converter (ADC) with Encoder

This block samples the incoming analog data with the clock signal provided by the CMU in order to generate a 4-bit output digital signal (Bit 0 – Bit 3) with MSB corresponding to Bit 3. The threshold voltages ($V_{th\,1}$ - $V_{th\,15}$) of the ADC can be adjusted through analog signals vrefcrl and vlsbcrl as shown in Table 1. As can be seen, vrefcrl shifts the DC levels of all the threshold voltages simultaneously by the same amount in relation to vcc and vlsbcrl alters the voltage range of the least significant bit (LSB) while also shifting the DC levels.

Table 1. Simulated ADC Threshold Control States

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vrefcrl. *mV*	vlsbcrl. *mV*	$V_{th\ 15}$, *mV*	$V_{th\ 8}$, *mV*	$V_{th\ 1}$, *mV*	$V_{th\ (X+1)} - V_{th\ X}$, *mV*
min (vcc – 960)	min (vcc – 700)	vcc-35	vcc-54	vcc-73	2.7
min (vcc – 960)	max (vcc – 260)	vcc-345	vcc-751	vcc-1157	58
max (vcc)	min (vcc – 700)	vcc-355	vcc-361	vcc-366	0.8
max (vcc)	max (vcc – 260)	vcc-665	vcc-1058	vcc-1450	56

If no external voltages are applied to vrefcrl and vlsbcrl, it is recommended to have both pins AC-terminated by 50*Ohm* resistors to vee through DC blocks! The corresponding default states are vrefcrl=vlsbcrl=vcc-0.48*V*.

Demultiplexer (4:16 DMX)

This block deserializes the 4-bit words from the ADC into 16-bit output words as shown in Table 2.

Table 2. Demultiplexer Bit Order

Serialized input words	First				Second				Third				Fourth			
ADC bits (3 is MSB)	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
DMX output bits	00	04	08	12	01	05	09	13	02	06	10	14	03	07	11	15

Clock Processor (Clk Proc)

To increase the adaptability of the designed ADC, a clock processor that provides a low-speed output clock signal with the options specified in Table 3, is included.

Table 3. Output Clock Options

External control signals			**Output clock signal**	
cosel1	cosel2	cosel3	**Speed**	**Inversion**
1	1	1	c4	Yes
1	1	0	c4	No
0	1	1	c8	Yes
0	1	0	c8	No
x	0	1	c16	Yes
x	0	0	c16	No

Digital to Analog Converter (DAC)

A DAC block is included to perform a quick test of the ADC's functionality. When activated by the external control signal (ondac="1"), it converts the digital data into a step-wise copy of the input signal that is sent to the output odp/odn through a linear differential output buffer LOB. The circuit is not consuming any power when disabled (ondac="0", default).

LVDS Output Buffers

The 16-bit differential digital data words q00p/q00n to q15p/q15n are delivered to the output through an array of proprietary low power LVDS buffers. The low speed differential clock clop/clon also utilizes a similar LVDS output buffer. The buffers satisfy all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995.

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TERMINAL FUNCTIONS

Pin #	Pin name	Pin type	Pin function	Termination or connection
1	vee	supply voltage	negative power supply	GND
2	vee	supply voltage	negative power supply	GND
3	q02p	LVDS output	Output data Bit 02, direct	Needs external 100*Ohm* between pins
4	q02n		Output data Bit 02, inverted	
5	vcc	supply voltage	positive power supply	
6	q01p	LVDS output	Output data Bit 01, direct	Needs external 100*Ohm* between pins
7	q01n		Output data Bit 01, inverted	
8	vcc	supply voltage	positive power supply	
9	q00p	LVDS output	Output data Bit 00, direct	Needs external 100*Ohm* between pins
10	q00n		Output data Bit 00, inverted	
11	vcc	supply voltage	positive power supply	
12	clop	LVDS output	LS output clock, direct	Needs external 100*Ohm* between pins
13	clon		LS output clock, inverted	
14	n/c		not used	
15	vee	supply voltage	negative power supply	GND
16	cosel1	CMOS input	LS output clock phase control	1*MOhm* to vee
17	cosel2	CMOS input	LS output clock phase control	1*MOhm* to vee
18	cosel3	CMOS input	LS output clock phase control	1*MOhm* to vee
19	lol	CMOS output	PLL no-lock indicator	
20	ftr		External filter connection	
21	vee	supply voltage	negative power supply	GND
22	ceoff	CMOS input	Clock multiplication/division mode	1*MOhm* to 2.5*V*
23	n/c		not used	
24	n/c		not used	
25	vcc	supply voltage	positive power supply	
26	vcc	supply voltage	positive power supply	
27	crn	LVDS input	LS reference input clock, direct	100*Ohm* between pins
28	crp		LS reference input clock, inverted	
29	vcc	supply voltage	positive power supply	
30	vee	supply voltage	negative power supply	GND
31	vee	supply voltage	negative power supply	GND
32	vcc	supply voltage	positive power supply	
33	cen	CML input	HS input clock, direct	50*Ohm* to vcc
34	cep	CML input	HS input clock, inverted	50*Ohm* to vcc
35	vcc	supply voltage	positive power supply	
36	vee	supply voltage	negative power supply	GND
37	vee	supply voltage	negative power supply	GND
38	vcc	supply voltage	positive power supply	

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Pin #	Pin name	Pin type	Pin function	**Termination or connection**
39	dn	Analog input	HS input data, direct	50*Ohm* to vcc
40	dp	Analog input	HS input data, inverted	50*Ohm* to vcc
41	vcc	supply voltage	positive power supply	
42	vee	supply voltage	negative power supply	GND
43	vee	supply voltage	negative power supply	GND
44	vcc	supply voltage	positive power supply	
45	n/c		not used	
46	res	CMOS input	Divider reset (active-high)	640*KOhm* to vee
47	ondac	CMOS input	DAC enable/disable	1*MOhm* to vee
48	vlsbcrl	Analog voltage	ADC threshold voltages controls	12*KOhm* to vcc
49	vrefcrl	Analog voltage		12*KOhm* to vcc
50	vee	supply voltage	negative power supply	GND
51	vee	supply voltage	negative power supply	GND
52	n/c		not used	
53	n/c		not used	
54	n/c		not used	
55	vcc	supply voltage	positive power supply	
56	odp	Analog output	DAC output signal, direct	50*Ohm* to vcc
57	odn	Analog output	DAC output signal, inverted	50*Ohm* to vcc
58	vee	supply voltage	negative power supply	GND
59	n/c		not used	
60	q15p	LVDS output	Output data Bit 15, direct	Needs external 100*Ohm* between pins
61	q15n		Output data Bit 15, inverted	
62	vcc	supply voltage	positive power supply	
63	q14p	LVDS output	Output data Bit 14, direct	Needs external 100*Ohm* between pins
64	q14n		Output data Bit 14, inverted	
65	vcc	supply voltage	positive power supply	
66	q13p	LVDS output	Output data Bit 13, direct	Needs external 100*Ohm* between pins
67	q13n		Output data Bit 13, inverted	
68	vcc	supply voltage	positive power supply	
69	q12p	LVDS output	Output data Bit 12, direct	Needs external 100*Ohm* between pins
70	q12n		Output data Bit 12, inverted	
71	vcc	supply voltage	positive power supply	
72	q11p	LVDS output	Output data Bit 11, direct	Needs external 100*Ohm* between pins
73	q11n		Output data Bit 11, inverted	
74	vee	supply voltage	negative power supply	GND
75	vee	supply voltage	negative power supply	GND
76	vcc	supply voltage	positive power supply	
77	q10p	LVDS output	Output data Bit 10, direct	Needs external 100*Ohm* between pins
78	q10n		Output data Bit 10, inverted	
79	vcc	supply voltage	positive power supply	

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Pin #	Pin name	Pin type	Pin function	Termination or connection
80	q09p	LVDS output	Output data Bit 09, direct	Needs external 100*Ohm* between pins
81	q09n		Output data Bit 09, inverted	
82	vcc	supply voltage	positive power supply	
83	q08p	LVDS output	Output data Bit 08, direct	Needs external 100*Ohm* between pins
84	q08n		Output data Bit 08, inverted	
85	vcc	supply voltage	positive power supply	
86	q07p	LVDS output	Output data Bit 07, direct	Needs external 100*Ohm* between pins
87	q07n		Output data Bit 07, inverted	
88	vcc	supply voltage	positive power supply	
89	q06p	LVDS output	Output data Bit 06, direct	Needs external 100*Ohm* between pins
90	q06n		Output data Bit 06, inverted	
91	vcc	supply voltage	positive power supply	
92	q05p	LVDS output	Output data Bit 05, direct	Needs external 100*Ohm* between pins
93	q05n		Output data Bit 05, inverted	
94	vcc	supply voltage	positive power supply	
95	q04p	LVDS output	Output data Bit 04, direct	Needs external 100*Ohm* between pins
96	q04n		Output data Bit 04, inverted	
97	vcc	supply voltage	positive power supply	
98	q03p	LVDS output	Output data Bit 03, direct	Needs external 100*Ohm* between pins
99	q03n		Output data Bit 03, inverted	
100	vcc	supply voltage	positive power supply	

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings presented in Table 4 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (vee).

Table 4. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vcc)		4.0	*V*
Power Consumption		4.0	*W*
RF Input Voltage Swing (SE)		1.4	*V*
Case Temperature		+100	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vcc	3. 4	3.5	3.6	*V*	±3%
vee		0.0		*V*	External ground
*I*vcc		1020		*mA*	
Power consumption		3.57		*W*	
Junction temperature	-25	50	125	*°C*	
Analog Input Data (dp/dn)					
Bandwidth	0.0		20	*GHz*	
CM Level	vcc-0.8		vcc	*V*	Must match for both inputs
Linearity range		±110		*mV*	Differential or SE, p-p
HS Input Clock (cep/cen)					
Frequency	DC		15	*GHz*	
Swing	0.2		0.8	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
Duty Cycle	40	50	60	*%*	
LS Reference Input Clock (crp/crn)					
Frequency	560		688	*MHz*	1/16 of VCO frequency
CM Level	0.2		vcc	*V*	
Voltage Swing	100		800	*mV*	Differential
Duty Cycle	40	50	60	*%*	
Output Data (q00p/q00n to q15p/q15n)					
Data Rate	DC		3.75	*Gbps*	
CM Level		1.2		*V*	Nominal for LVDS interface
Amplitude range	250		350	*mV*	
Rise/Fall Times		TBD		*ps*	20%-80%
LS Output Clock (clop/clon)					
Frequency	*f*/4	*f*/8	*f*/16	*GHz*	Selectable. Here *f* is the PLL or HS input clock frequency
CM Level		1.2		*V*	Nominal for LVDS interface
Amplitude range	250		350	*V*	
Jitter		TBD		*ps*	
Duty Cycle		50		*%*	
DAC Output (odp/odn)					
Voltage Swing	250		350	*mV*	Single-ended. p-p
CM Level	vcc-(voltage swing)/2			*V*	
Analog Control Signals (vrefcrl, vlsbcrl)					
Voltage range				*V*	See Table 1
CMOS Control Signals (cosel1, cosel2, cosel3, ceoff, res, ondac)					
Logic "1" level	vee+2.3		vee+2.5	*V*	
Logic "0" level			vee+0.2	*V*	
Frequency			3.5	*GHz*	

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ELECTRICAL SPECIFICATIONS

Parameter	Conditions	Min	Typical	Max	Units
ENOB (5GS/s)	fin = 3.9GHz		3.39		*bits*
ENOB (10GS/s)	fin = 7.8GHz		3.23		*bits*
SFDR (5GS/s)	fin = 3.9GHz		30.13		*dBFS*
SFDR (10GS/s)	fin = 7.8GHz		28.78		*dBFS*
SINAD (5GS/s)	fin = 3.9GHz		-22.15		*dB*
SINAD (10GS/s)	fin = 7.8GHz		-21.19		*dB*
DNL		-0.2		0.2	*lsbs*
INL		-0.2		0.2	*lsbs*

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PACKAGE INFORMATION

The chip die is housed in a custom 100-pin CQFP package shown in Fig. 3.

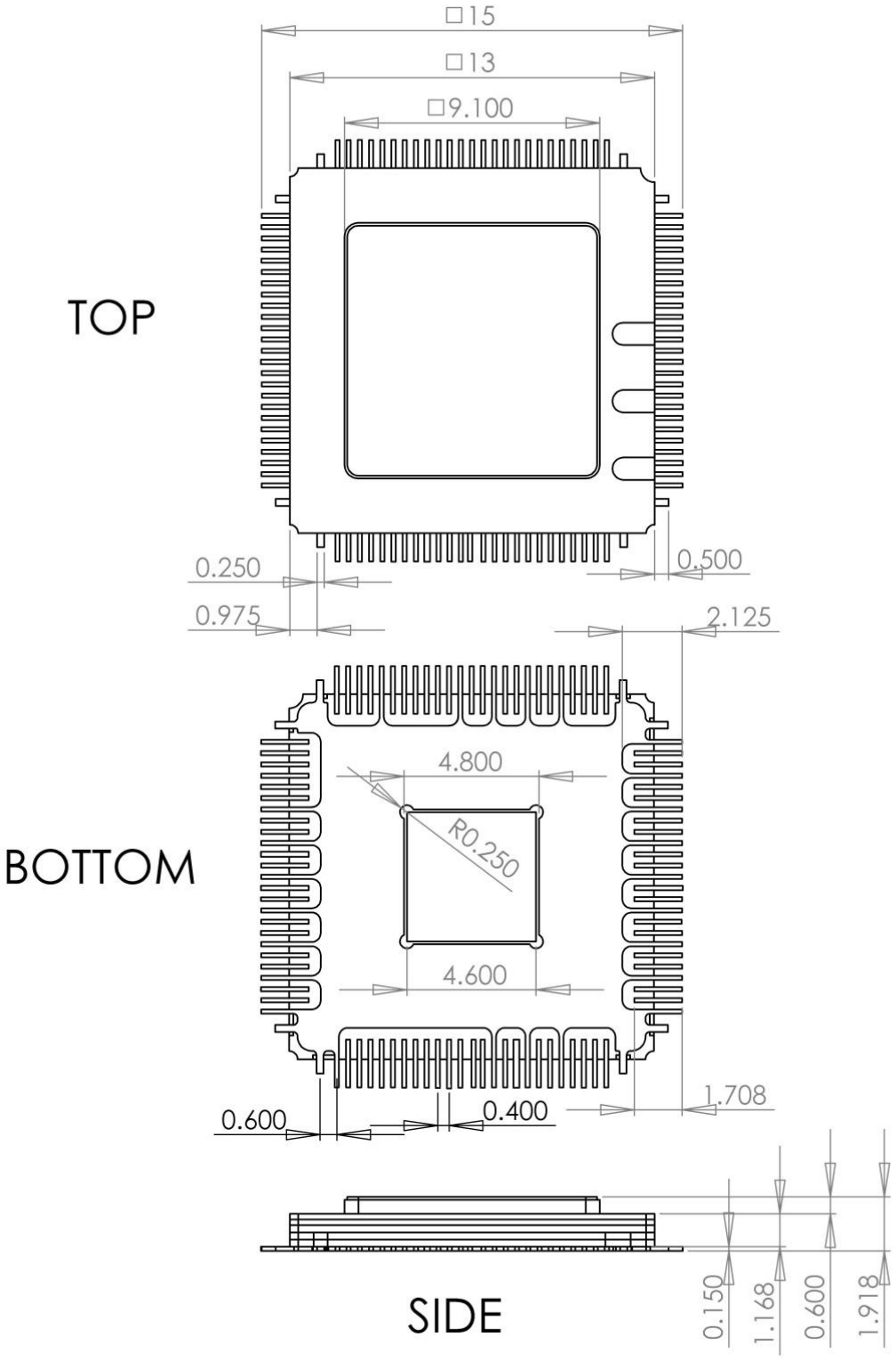

Fig. 3. CQFP 100-Pin Package Drawing (All Dimensions in mm)

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The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is power for a positive supply.

The part's identification label is ASNT7120A-KMA. The first 9 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all six substances.

REVISION HISTORY

Revision	Date	Changes
1.4.1	09-2015	Removed cpcsel function (Pinout diagram, block diagram, description, Terminal Functions table, Electrical Characteristics table)
1.3.1	08-2015	Added Electrical Specifications table
1.2.1	07-2015	Updated title Updated Absolute Maximum Ratings section Revised Electrical Characteristics table Updated Package Information section
1.1.1	04-2015	Corrected pin out diagram (cpcsel pin name) Corrected description Corrected description of ADC threshold controls Modified Terminal Functions table
1.0.1	03-2015	Updated block diagram Corrected description Corrected power consumption value Corrected absolute maximum power
1.0.0	08-2014	First release