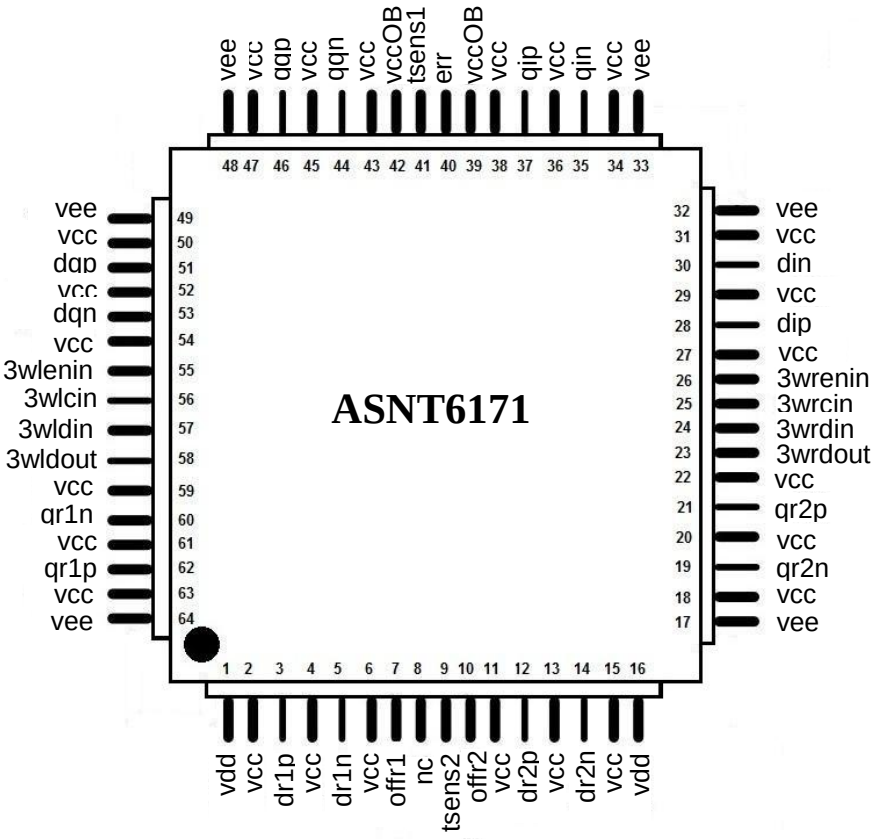
ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
27 Via Porto Grande, Rancho Palos Verdes, CA 90275

Offices: 310-377-6029 / 310-803-9284 Fax: 310-377-9940
www.adsantec.com

ASNT6171-KMO
DC-20*Gbps*/10*GHz* 15-tap Analog FIR Filter

- Dual FIR filter with 15 fully controlled taps for analog signals
- High bandwidth DC-20*Gbps* / 10*GHz*
- Total gain up to 14*dB*
- Dual-port 3-wire SPI for tap weight and sign adjustment
- Additional frequency response and gain adjustment through the SPI
- Fully differential CML-type analog input interface
- Fully differential CML-type analog output interface
- Independent power supplies for analog and digital sections
- Power consumption: <2.65*W*
- Fabricated in SiGe for high performance, yield, and reliability
- Limited temperature variation over industrial temperature range
- Die size 5.8x5.8mm^2
- Optional custom CQFP 64-pin package



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DESCRIPTION

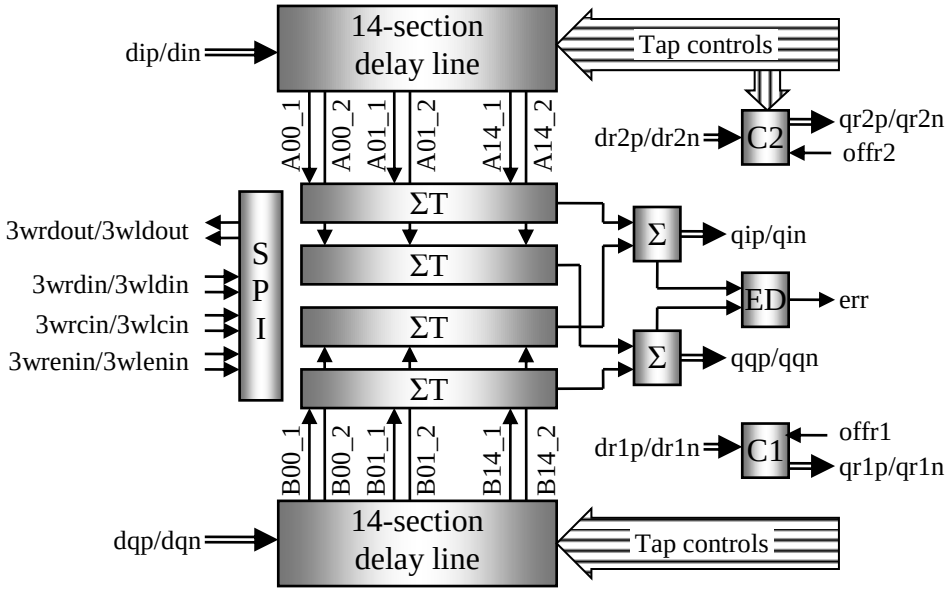

Fig. 1. Functional Block Diagram

The ASNT6171-KMO part is a dual 15-tap FIR filter for processing of two analog signals dip/din and dqp/dqn. It includes two passive delay lines with 14 matching sections and three loss-compensating buffers in each one. The buffers feature gain and frequency response adjustment. The signals from all 15 nodes of both delay lines are delivered to 4 summation blocks (ΣT) through taps. Each tap in both delay lines includes two buffers with individually controlled weight and sign.

The part also includes two output summation blocks (Σ) that allow for mixing of equalized signals from both channels. The resulting signals are delivered to two output analog ports qip/qin and qqp/qqn. The output buffers may have a separate supply voltage for adjustment of the output common-mode voltage level. They also have additional adjustments of gain and frequency response.

The equalized signals are also processed by an error detector block (ED) to produce an error signal that indicates the signal deviation from an ideal pulse shape.

The part includes two calibration blocks for initial calibration of gain and frequency response in the output buffers (C1) and in taps (C2).

All analog input/output ports have internal 50*Ohm* terminations to positive supply rails. The output ports require external 50*Ohm* DC terminations to the same supply rails or AC terminations to ground.

All functions are controlled through a dual 3-wire SPI interface that has two 4-pin ports. Both ports support standard 3-wire slave functionality.

The chip includes two temperature sensors implemented as large diodes with their cathodes connected to vee and their anodes connected to tsens1 and tsens2 ports. The sensors represent temperatures at the top and the bottom of the die respectively.

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Delay Lines

Each delay line block includes 14 passive delay sections implemented as transmission lines, an input buffer (IB) before the first delay section, a loss-compensating buffer after the fourth delay section (B5), and a loss-compensating buffer after the ninth delay section (B10). All buffers feature independent adjustments of gain and peaking (or frequency response) through the 3-wire interface. The analog signal to the input buffers is delivered through differential interfaces dip/din and dqp/dqn.

The inputs of the delay lines, and the outputs of all their delay sections are connected to the inputs of 15 pairs of matching tap buffers. In each pair, the output of the first buffer (Axx_1 or Bxx_1) is connected to one tap summation block, and the output of the second buffer (Axx_2 or Bxx_2) is connected to the other tap summation block. This provides two matching outputs from each delay line. Each tap buffer features an independent adjustment of its gain, and the output polarity selection controlled through the 3-wire interface.

Four tap summation blocks are implemented as short transmission lines connected to two output summation blocks.

With peaking in the input and loss-compensating buffers set to its average value, the typical gain vs. frequency characteristic of one tap is plotted in Fig. 2.

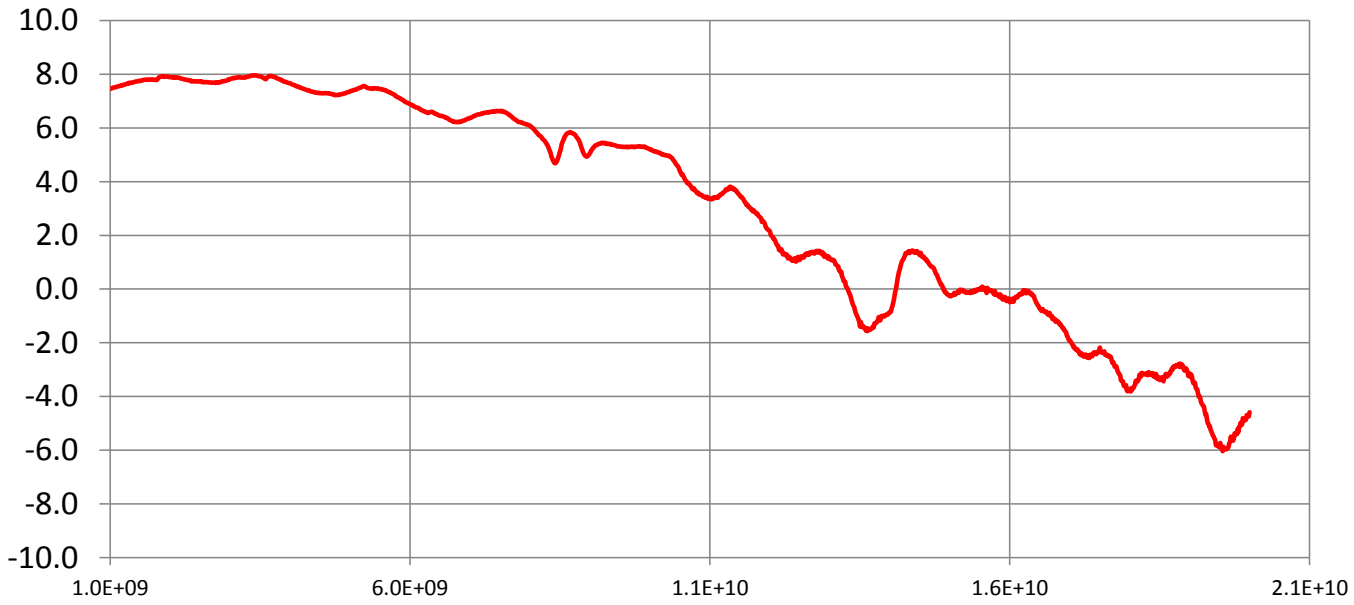

Fig. 2. Gain of one tap

The typical group delay variation of one tap vs. frequency is plotted in Fig. 3.

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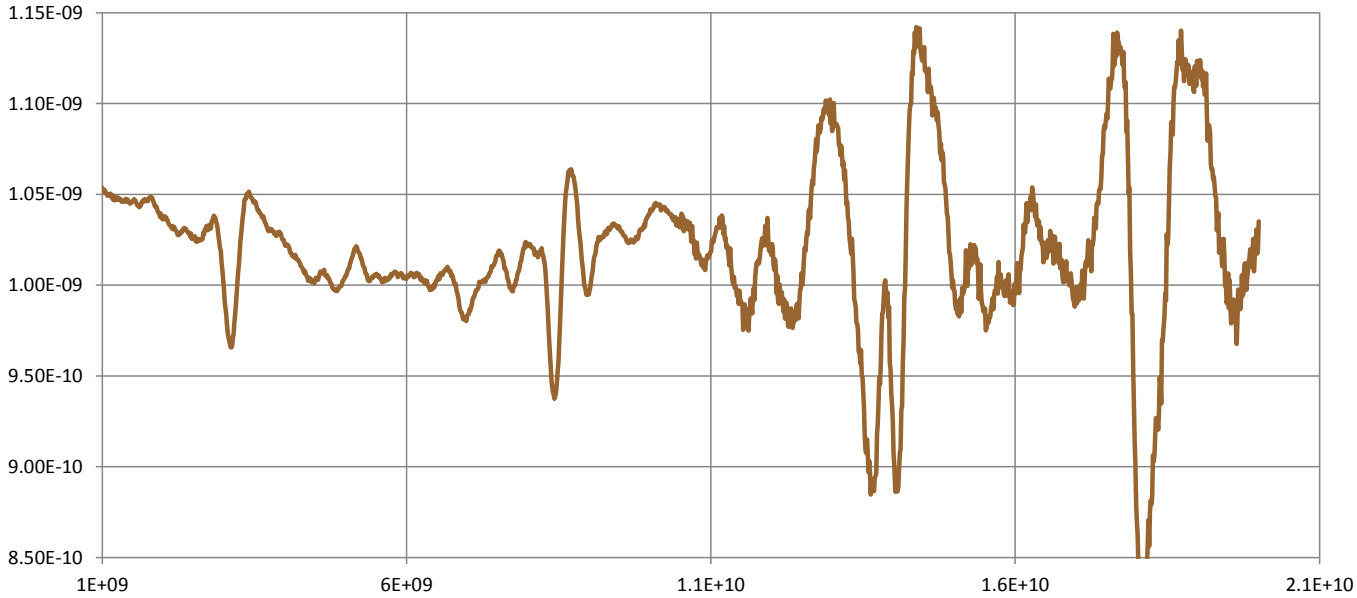

Fig. 3. Group Delay of one tap

Output Summation Blocks and Output Buffers

Each output summation block is an analog current combiner that mixes one signal from one delay line block with one signal from another delay line block. The combined signals are delivered to differential output ports qip/qin and qqp/qqn through output buffers.

Error Detector

The two combined signals before the output buffers are also delivered to the error detector block. The error detector performs the function $ERR = S^2 - \overline{(S^2)}$ on each of the input signals. The *ERR* equals 0 for an ideal signal *S* and increases with the signal shape deviation from the ideal.

The error signals for both input signals are combined together for sensitivity improvement and are then delivered to the single-ended output port err.

Calibration Blocks

The chip includes two calibration blocks that allow for controlled initial setting of all internal buffers.

The first calibration block (C1) is an exact copy of the output summation blocks and buffers. It is also controlled by the same signals from the 3-wire interface. Measuring parameters of the signals at its input dr1p/dr1n, and output qr1p/qr1n allows for the initial gain and peaking settings of the corresponding stages.

The second calibration block (C2) includes the same stages as C1 as well as an exact copy of a tap buffer. Measuring parameters of the signals at its input dr2p/dr2n, and output qr2p/qr2n allows for the initial gain and peaking settings of the tap buffers.

The calibration block can be enabled or disabled by CMOS control signals offr1 and offr2 respectively. The calibration procedures are described in detail in the application notes for this part.

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3-Wire SPI Control Block

The interface incorporates two ports (right and left) that include data inputs 3wrdin and 3wldin, clock inputs 3wrcin and 3wlcin, enable inputs 3wrenin and 3wlenin, and data outputs 3wrdout and 3wldout. Each port controls certain internal blocks as described below.

Left-Side SPI Port

Table 1 refers to the left-side SPI port.

Table 1. Left CDE SPI Data Transfer Protocol

Byte #	Bit #	Bit order	Signal name	Signal function
1	From 1	LSB	crlgn	X and Y channels Input buffers gain control
	to 8	MSB		
2	1	sign	crlyi0	Tap0 YI buffer gain control
	From 2	LSB		
	to 8	MSB		
3	1	sign	crlyq0	Tap0 YQ buffer gain control
	From 2	LSB		
	to 8	MSB		
4	1	sign	crlyi1	Tap1 YI buffer gain control
	From 2	LSB		
	to 8	MSB		
5	1	sign	crlyq1	Tap1 YQ buffer gain control
	From 2	LSB		
	to 8	MSB		
6	1	sign	crlyi2	Tap2 YI buffer gain control
	From 2	LSB		
	to 8	MSB		
7	1	sign	crlyq2	Tap2 YQ buffer gain control
	From 2	LSB		
	to 8	MSB		
8	1	sign	crlyi3	Tap3 YI buffer gain control
	From 2	LSB		
	to 8	MSB		
9	1	sign	crlyq3	Tap3 YQ buffer gain control
	From 2	LSB		
	to 8	MSB		
10	From 1	LSB	crlg5	X and Y channels buffer5’s gain control
	to 8	MSB		
11	1	sign	crlyi4	Tap4 YI buffer gain control
	From 2	LSB		
	to 8	MSB		
12	1	sign	crlyq4	Tap4 YQ buffer gain control
	From 2	LSB		
	to 8	MSB		

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Byte #	Bit #	Bit order	Signal name	Signal function
13	1	sign	crlyi5	Tap5 YI buffer gain control
	From 2	LSB		
	to 8	MSB		
14	1	sign	crlyq5	Tap6 YQ buffer gain control
	From 2	LSB		
	to 8	MSB		
15	1	sign	crlyi6	Tap6 YI buffer gain control
	From 2	LSB		
	to 8	MSB		
16	1	sign	crlyq6	Tap6 YQ buffer gain control
	From 2	LSB		
	to 8	MSB		
17	1	sign	crlyi7	Tap7 YI buffer gain control
	From 2	LSB		
	to 8	MSB		
18	1	sign	crlyq7	Tap7 YQ buffer gain control
	From 2	LSB		
	to 8	MSB		
19	1	sign	crlyi8	Tap8 YI buffer gain control
	From 2	LSB		
	to 8	MSB		
20	1	sign	crlyqi8	Tap8 YQ buffer gain control
	From 2	LSB		
	to 8	MSB		
21	From 1			Not used
	to 8			
22	From 1	LSB	crlg10	X and Y channels buffer10’s gain control
	to 8	MSB		
23	1	sign	crlyi9	Tap9 YI buffer gain control
	From 2	LSB		
	to 8	MSB		
24	1	sign	crlyq9	Tap9 YQ buffer gain control
	From 2	LSB		
	to 8	MSB		
25	1	sign	crlyi10	Tap10 YI buffer gain control
	From 2	LSB		
	to 8	MSB		
26	1	sign	crlyq10	Tap10 YQ buffer gain control
	From 2	LSB		
	to 8	MSB		
27	1	sign	crlyi11	Tap11 YI buffer gain control
	From 2	LSB		
	to 8	MSB		

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Byte #	Bit #	Bit order	Signal name	Signal function
28	1	sign	crlyq11	Tap11 YQ buffer gain control
	From 2	LSB		
	to 8	MSB		
29	1	sign	crlyi12	Tap12 YI buffer gain control
	From 2	LSB		
	to 8	MSB		
30	1	sign	crlyq12	Tap12 YQ buffer gain control
	From 2	LSB		
	to 8	MSB		
31	1	sign	crlyi13	Tap13 YI buffer gain control
	From 2	LSB		
	to 8	MSB		
32	1	sign	crlyq13	Tap13 YQ buffer gain control
	From 2	LSB		
	to 8	MSB		
33	1	sign	crlyi14	Tap14 YI buffer gain control
	From 2	LSB		
	to 8	MSB		
34	1	sign	crlyq14	Tap14 YQ buffer gain control
	From 2	LSB		
	to 8	MSB		

Right-Side SPI Port

Table 2 refers to the right-side SPI port.

Table 2. Right CDE SPI Data Transfer Protocol

Byte #	Bit #	Bit order	Signal name	Signal function
1	From 1	LSB	crlpk	X and Y channels Input buffers peaking control
	to 8	MSB		
2	1	sign	crlxi0	Tap0 XI buffer gain control
	From 2	LSB		
	to 8	MSB		
3	1	sign	crlxq0	Tap0 XQ buffer gain control
	From 2	LSB		
	to 8	MSB		
4	1	sign	crlxi1	Tap1 XI buffer gain control
	From 2	LSB		
	to 8	MSB		
5	1	sign	crlxq1	Tap1 XQ buffer gain control
	From 2	LSB		
	to 8	MSB		

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Byte #	Bit #	Bit order	Signal name	Signal function
6	1	sign	crlxi2	Tap2 XI buffer gain control
	From 2	LSB		
	to 8	MSB		
7	1	sign	crlxq2	Tap2 XQ buffer gain control
	From 2	LSB		
	to 8	MSB		
8	1	sign	crlxi3	Tap3 XI buffer gain control
	From 2	LSB		
	to 8	MSB		
9	1	sign	crlxq3	Tap3 XQ buffer gain control
	From 2	LSB		
	to 8	MSB		
10	From 1	LSB	crlp5	X and Y channels buffer5's peaking control
	to 8	MSB		
11	1	sign	crlxi4	Tap4 XI buffer gain control
	From 2	LSB		
	to 8	MSB		
12	1	sign	crlxq4	Tap4 XQ buffer gain control
	From 2	LSB		
	to 8	MSB		
13	1	sign	crlxi5	Tap5 XI buffer gain control
	From 2	LSB		
	to 8	MSB		
14	1	sign	crlxq5	Tap6 XQ buffer gain control
	From 2	LSB		
	to 8	MSB		
15	1	sign	crlxi6	Tap6 XI buffer gain control
	From 2	LSB		
	to 8	MSB		
16	1	sign	crlxq6	Tap6 XQ buffer gain control
	From 2	LSB		
	to 8	MSB		
17	1	sign	crlxi7	Tap7 XI buffer gain control
	From 2	LSB		
	to 8	MSB		
18	1	sign	crlxq7	Tap7 XQ buffer gain control
	From 2	LSB		
	to 8	MSB		
19	1	sign	crlxi8	Tap8 XI buffer gain control
	From 2	LSB		
	to 8	MSB		
20	1	sign	crlxqi8	Tap8 XQ buffer gain control
	From 2	LSB		

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Byte #	Bit #	Bit order	Signal name	Signal function
	to 8	MSB		
21	From 1	LSB	crlout	Q and I output buffers gain control
	to 8	MSB		
22	From 1	LSB	crlp10	X and Y channels buffer10's peaking control
	to 8	MSB		
23	1	sign	crlxi9	Tap9 XI buffer gain control
	From 2	LSB		
	to 8	MSB		
24	1	sign	crlxq9	Tap9 XQ buffer gain control
	From 2	LSB		
	to 8	MSB		
25	1	sign	crlxi10	Tap10 XI buffer gain control
	From 2	LSB		
	to 8	MSB		
26	1	sign	crlxq10	Tap10 XQ buffer gain control
	From 2	LSB		
	to 8	MSB		
27	1	sign	crlxi11	Tap11 XI buffer gain control
	From 2	LSB		
	to 8	MSB		
28	1	sign	crlxq11	Tap11 XQ buffer gain control
	From 2	LSB		
	to 8	MSB		
29	1	sign	crlxi12	Tap12 XI buffer gain control
	From 2	LSB		
	to 8	MSB		
30	1	sign	crlxq12	Tap12 XQ buffer gain control
	From 2	LSB		
	to 8	MSB		
31	1	sign	crlxi13	Tap13 XI buffer gain control
	From 2	LSB		
	to 8	MSB		
32	1	sign	crlxq13	Tap13 XQ buffer gain control
	From 2	LSB		
	to 8	MSB		
33	1	sign	crlxi14	Tap14 XI buffer gain control
	From 2	LSB		
	to 8	MSB		
34	1	sign	crlxq14	Tap14 XQ buffer gain control
	From 2	LSB		
	to 8	MSB		

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Power supply configuration

The part operates from three positive power supplies related to a common ground vee.

The main supply is vcc. It powers all analog blocks except for the output buffers.

The second supply vccOB powers the output buffers and can be used for the output common mode voltage adjustment. If such adjustment is not required, vccOB can be shorted to vcc.

The third supply vdd is used for the internal CMOS circuits of the SPI.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 3 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vee).

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vcc)		+3.6	*V*
Power Consumption		3.0	*W*
RF Input Voltage Swing (SE)		0.5	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+3.3*V*)	2, 4, 6, 11, 13, 15, 18, 20, 22, 27, 29, 31, 34, 36, 38, 43, 45, 47, 50, 52, 54, 59, 61, 63
vee	Negative power supply (GND or 0*V*)	17, 32, 33, 48, 49, 64
vdd	Positive power supply (+1.3*V*)	1, 16
vccOB	Positive power supply (+3.3*V*)	39, 42
nc	Not connected	8

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TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
dip	28	Analog input	CML-type differential data ports with internal SE 50*Ohm* termination to VCC
din	30		
dqp	51		
dqn	53		
dr1p	3		
dr1n	5		
dr2p	12		
dr2n	14		
qip	37	Analog output	CML-type differential data ports with internal SE 50*Ohm* termination to VCC. Require external SE 50*Ohm* termination to VCC.
qin	35		
qqp	46		
qqn	44		
qr1p	62		
qr1n	60		
qr2p	21		
qr2n	19		
Controls			
offr1	7	3.3*V* CMOS input	C1 activation (default: high, C1 is off; active: low, C1 is on)
offr2	10		C2 activation (default: high, C2 is off; active: low, C2 is on)
err	40	Analog output	Error signal high-impedance output port
tsens1	41	Current-sinking outputs	Connected to anodes of temperature-sensing diodes
tsens2	9		
3-Wire Controls			
3wrdin	24	1.2*V* CMOS input	Right-side data input
3wldin	57		Left-side data input
3wrcin	25		Right-side clock input
3wlcin	56		Left-side clock input
3wrenin	26		Right-side enable input
3wlenin	55		Left-side enable input
3wrdout	23	1.2*V* CMOS output	Right-side data output
3wldout	58		Left-side data output

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vcc	3.1	3.3	3.5	*V*	±6% , analog supply
vccOB	3.1	3.3	3.6	*V*	analog supply
vdd		1.3		*V*	±6%, digital supply
vee		0.0		*V*	External ground
*I*vcc			800	*mA*	
Power consumption			2.64	*W*	
Junction temperature	-25	50	125	*°C*	
Analog Input Data (dip/din, dqp/dqn)					
Frequency	DC		10	*GHz*	
Swing	0.02		0.1	*mV*	Differential or SE, p-p
S11		-12		*dB*	at 10GHz
CM Voltage Level		vcc		*V*	Must match for both inputs
Analog Output Data (qip/qin, qqp/qqn)					
Frequency	DC		18	*GHz*	
Swing		220		*mV*	on each SE output
S22		-12		*dB*	at 10GHz
CM Voltage Level		vccOB-0.35		*V*	
3-Wire Interface Ports					
Clock frequency			50	*MHz*	
Low logic level		0		*V*	
High logic level		1.2		*V*	

PACKAGE INFORMATION

The chip die is housed in a custom 64-pin CQFP package. The dimensioned drawings are shown in Fig. 4.

The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT6171-KMO. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all six substances.

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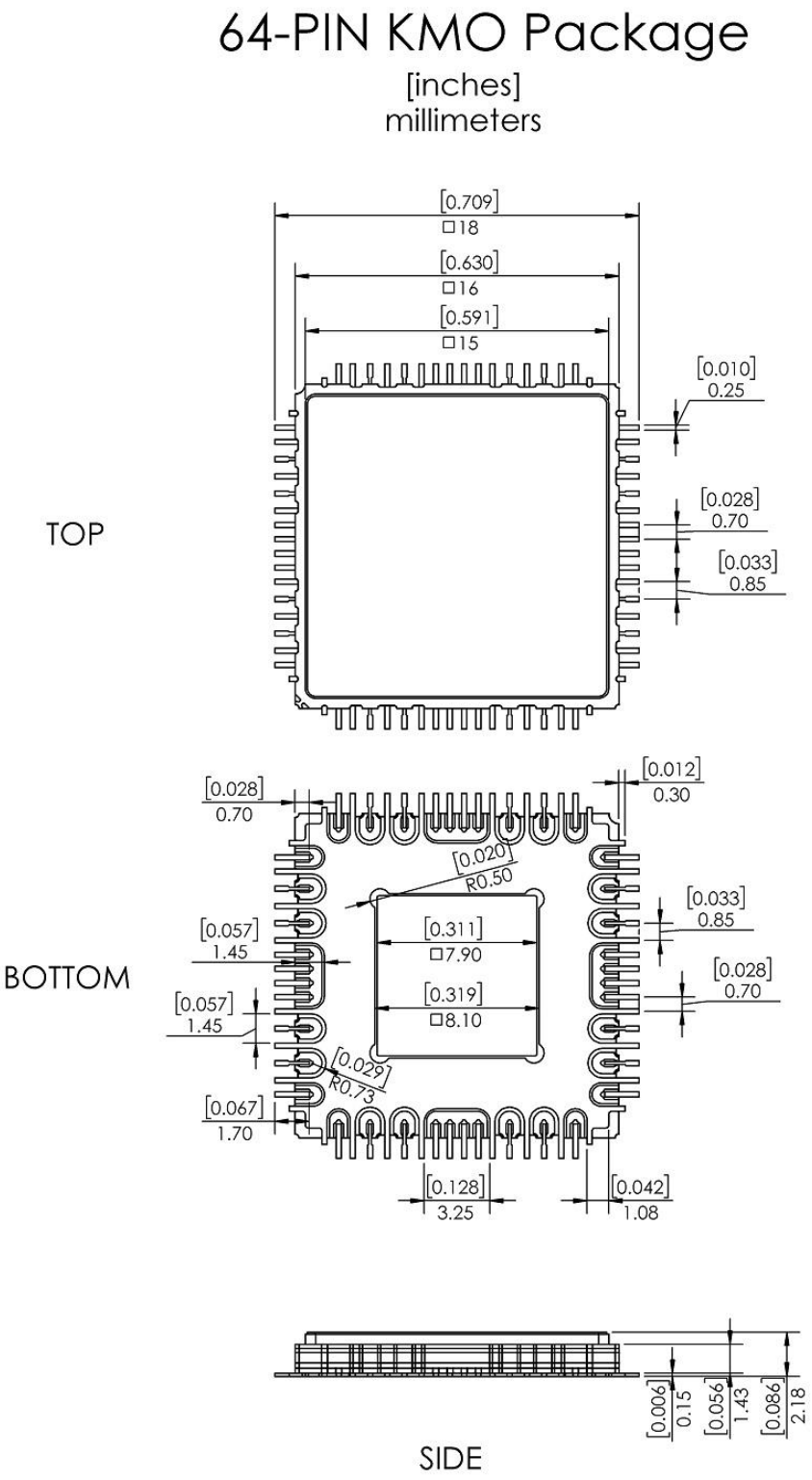

Fig. 4. CQFP 64-Pin Package Drawing (All Dimensions in mm)

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REVISION HISTORY

Revision	Date	Changes
1.0.1	12-2016	First release
0.2.1	08-2016	Updated title Corrected Package information section
0.1.1	08-2016	Added pin out diagram Corrected block diagram Corrected description Added Power Supply Configuration Added Absolute Maximum Ratings Added Package Information
0.0.1	07-2016	Preliminary release