ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
27 Via Porto Grande, Rancho Palos Verdes, CA 90275

Offices: 310-377-6029 / 310-803-9284 Fax: 310-377-9940
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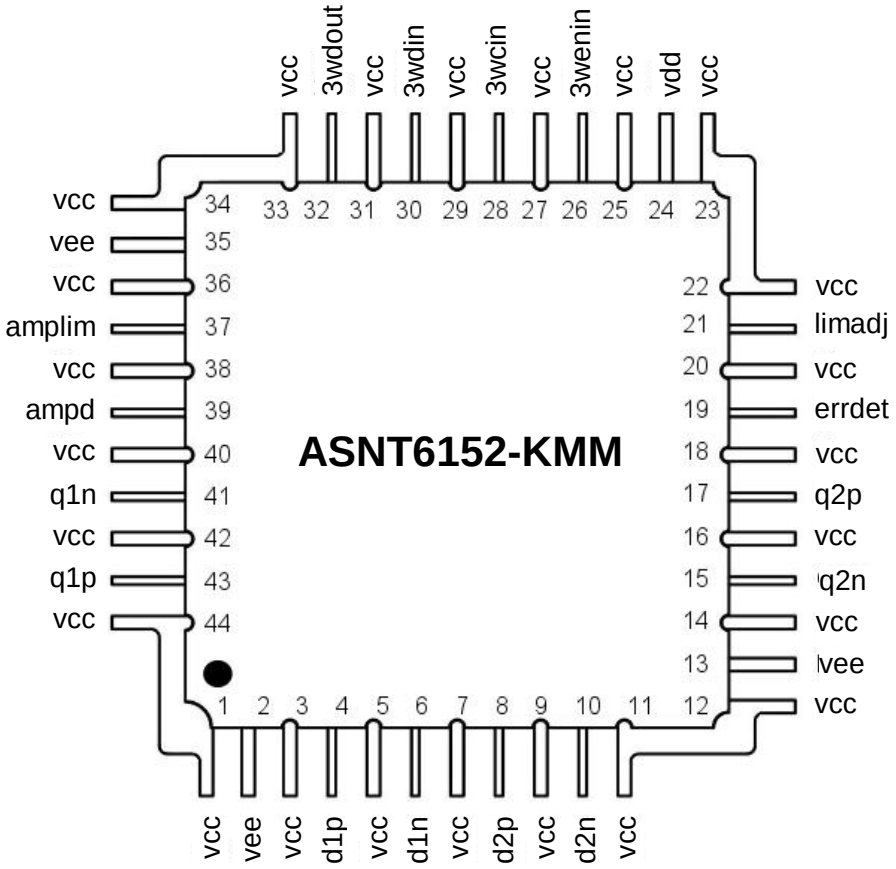
ASNT6152-KMM
8-28*Gbps* Dual CTLE with Error Detection/Pre-emphasis

- High-speed adjustable linear equalizer
- Two independent channels and two independent equalization stages per channel
- High-speed CMOS 3-wire interface for digital controls
- Self-adjusted 0*dB* DC gain
- Additional manual adjustment of DC gain through 3-wire interface
- Error detector in the first channel
- Adjustable error detector output range through 3-wire interface
- Fully differential CML-type analog input and output interface
- Two power supplies for the analog section and 3-wire interface
- Average power consumption with/without error detector: 1.4*W*/1.0*W*
- Fabricated in SiGe for high performance, yield, and reliability
- Limited temperature variation over industrial temperature range
- Die size 1.2x1.2mm^2
- Optional custom CQFP 44-pin package



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DESCRIPTION

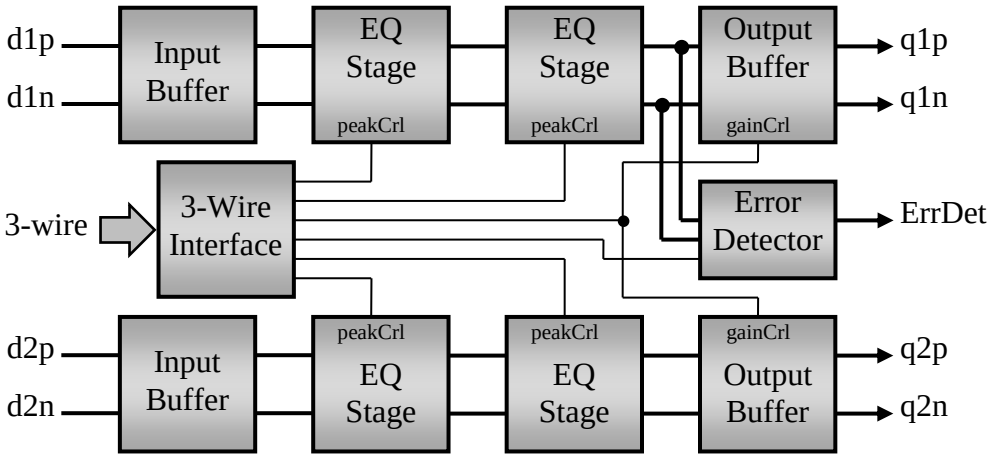

Fig. 1. Functional Block Diagram

The ASNT6152-KMM shown in Fig. 1 is an adaptive continuous-time linear equalizer (CTLE) with two independently controlled analog data channels, each channel with two identical and independently controlled equalization stages. The DC-gain in the equalization stages is automatically adjusted to 0*dB*. The DC-gain of the Output Buffer (OB) can be externally adjusted.

The first channel of the ADE features a built-in Error Detector (ED) that generates an output signal proportional to the absolute value of the difference between a recovered signal and an ideal signal. The ED can be turned off to save power.

The part's I/Os support CML-type differential interface with on-chip 50*Ohm* termination to vcc. External 50*Ohm* termination is also required. AC-coupling for both analog data channels is required.

All operational modes of the chip are controlled through a high-speed 3-wire serial interface (see **3-Wire Interface Control Block**).

The part operates with a positive supply vcc = +3.3*V* for the analog section, and a digital supply vdd = +1.3*V* for the SPI interface. The negative supply rail vee should be connected to external ground.

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Equalization Stages

The bandwidth of the ADE at minimum and maximum equalization is shown in Fig. 2.

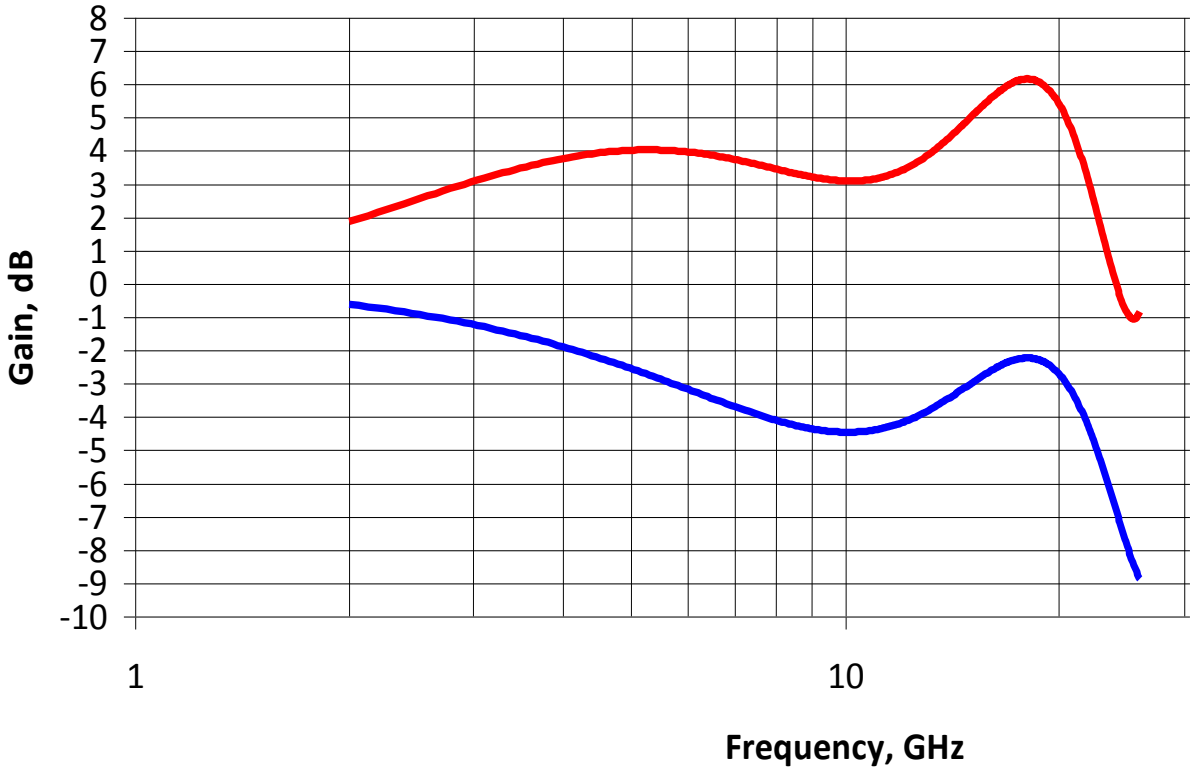

Fig. 2. ADE Bandwidth at Minimum Equalization (Blue) and Maximum Equalization (Red)

Total peaking of two equalization stages is shown in Fig. 3.

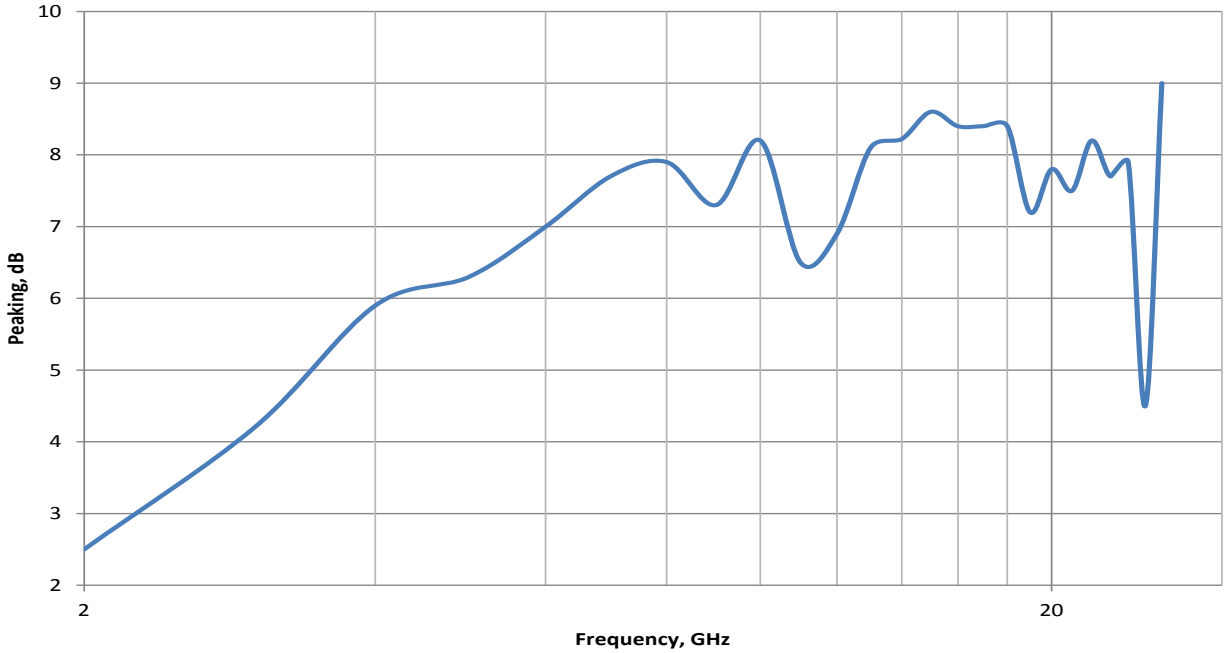

Fig. 3. Maximum Peaking of Two Equalization Stages

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3-Wire Interface Control Block

The interface supports high clock frequencies. The total reconfiguration time does not exceed 140*ns* from the external assignment of new control signals to the final settling of the internal controlled blocks.

The bit map of the interface is shown in Table 1

Table 1. 3-Wire Interface Bit Map

Byte #	Bit #	Bit order	Signal name	Signal function
1	From 1	LSB	e1ch1	Channel 1 Stage 1 EQ control
	to 8	MSB		
2	From 1	LSB	e2ch1	Channel 1 Stage 2 EQ control
	to 8	MSB		
3	From 1	LSB	e1ch2	Channel 2 Stage 1 EQ control
	to 8	MSB		
4	From 1	LSB	e2ch2	Channel 2 Stage 2 EQ control
	to 8	MSB		
5	From 1	LSB	del	Error Detector delay control
	to 8	MSB		
6	1	MSB	on_fb	Feedback switch: “1” – on, “0” - off
	From 2	LSB	amp	Output Buffer gain control
	to 8	2nd MSB		
7	1	MSB	on_ed	Error Detector switch: “1” – on, “0” - off
	From 2	LSB	eda	Error Detector gain control
	to 8	2nd MSB		

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TERMINAL FUNCTIONS

TERMINAL			Description
Name	**No.**	**Type**	
High-Speed I/Os			
d1p	4	CML-type Analog Inputs	Differential high-speed channel 1 data inputs
d1n	6		
d2p	8		Differential high-speed channel 2 data inputs
d2n	10		
q1p	43	CML-type Analog Outputs	Differential high-speed channel 1 data outputs
q1n	41		
q2p	17		Differential high-speed channel 2 data outputs
q2n	15		
Low-Speed I/Os			
3wenin	26	1.2*V* CMOS Inputs	Enable input signal for 3-wire interface
3wcin	28		Clock input signal for 3-wire interface
3wdin	30		Data input signal for 3-wire interface
3wdout	32	1.2*V* CMOS Output	Data output signal for 3-wire interface
errdet	19	CMOS Output	Error Detector output voltage
amplim	37		Error detector limited signal amplitude indicator
ampd	39		Error detector linear signal amplitude indicator
limadj	21	CMOS I/O	Error detector limiting voltage swing adjustment

Supply And Termination Voltages		
Name	**Description**	**Pin Number**
vdd	+1.2*V* positive power supply Negative pin to vee	24
vee	Ground	2, 13, 35
vcc	+3.3*V* positive power supply Negative pin to vee	1, 3, 5, 7, 9, 11, 12, 14, 16, 18, 20, 22, 23, 25, 27, 29, 31, 33, 34, 36, 38, 40, 42, 44

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 2 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vee).

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Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units
Digital Supply Voltage (vdd)		1.5	*V*
Analog Supply Voltage (vcc)		3.6	*V*
Power Consumption		1.6	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee		0.0		*V*	External ground
vdd	1.2		1.4	*V*	vdd pin to vee
vcc	3.1	3.3	3.5	*V*	vcc pin to vee
I_{vdd}		~0		*mA*	Depending on the state of the Error Detector (on or off)
I_{vcc}	300		410	*mA*	
Power Consumption	1.0		1.4	*W*	
Junction temperature	0	50	100	*°C*	
Data input (d1p/d1n, d2p/d2n)					
Data Rate	8		28	*Gb/s*	
SE Swing		220		*mV*	Peak-to-peak
CM Level		N/A			Only AC-coupled allowed
Data output (q1p/q1n, q2p/q2n)					
Rate	8		28	*Gb/s*	
SE Swing		220		*mV*	Peak-to-peak
CM Level		TBD		*V*	Depends on the amplitude
Error Detector output (errdet)					
Max. Swing		1		*V*	Adjustable via 3-w interface
3-Wire Interface Port					
Clock frequency			50	*MHz*	
Low logic level		0		*V*	
High logic levely		1.2		*V*	

PACKAGE INFORMATION

The chip die is housed in a custom, 44-pin CQFP package shown in Fig. 4. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

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The part's identification label is ASNT6152-KMM. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all six substances.

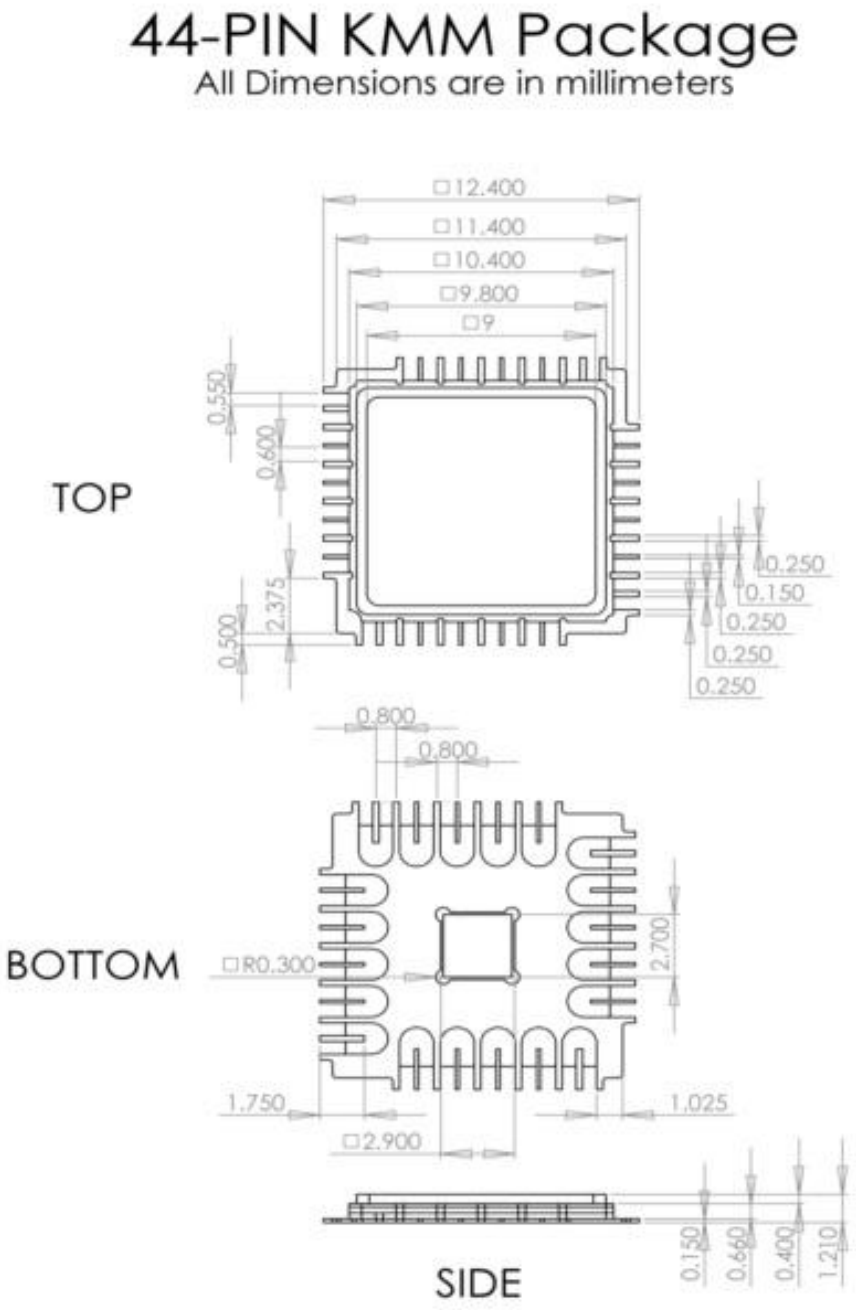

Fig. 4. Package Drawing

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REVISION HISTORY

Revision	Date	Changes
1.0.1	01-2017	First release
0.1.1	08-2016	Added pin out diagram Corrected description Corrected Terminal Functions table Added 3-wire interface speed to Electrical Characteristics
0.0.1	06-2016	Preliminary release