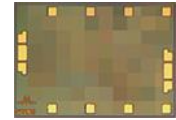


## BROADBAND AMPLIFIER

## AMM-6702

The AMM-6702 is a broadband MMIC LO buffer amplifier that efficiently provides high gain and output power over a 20-55 GHz frequency band. It is designed to provide a strong, flat output power response when driven with an input power at 0 dBm. It has built-in DC blocking capacitors on the input and output.



Bare Die

### Features

- High 25+ dB Gain
- Strong, Flat 20+ dBm Output Power Response
- High 20%+ PAE
- Unconditionally Stable

**Electrical Specifications** - Specifications measured in a 50-Ohm system.

Parameter	Frequency (GHz)	Typ	Min
Saturated Output Power (dBm)	20 to 55	+22	+17
Small Signal Gain (dB)		28	19
Input Return Loss (dB)		10	5
Output Return Loss (dB)		12	5
Noise Figure (dB)		6	
Bias Requirements, External (mA) <sup>1</sup> Vd: +3.0 / Vg: -0.6 Volts Vd: +3.0 / Vg: -0.5 Volts			130 180

<sup>1</sup> under no RF input power

### Part Number Options

Model Number	Description	Green Status	Product Lifecycle	Export Classification
AMM-6702CH	Chip	RoHS	Active	3A001.b.2.f

**BROADBAND AMPLIFIER**

**AMM-6702**

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Frequency 20 to 55 GHz

Functional Diagram

Bias Circuitry TBD



**Biasing and Operation**

**RF In / RF Out** – Input and output signals should be connected by 50 ohm microstrip or coplanar traces to well matched 50 ohm sources and loads. DC blocking capacitors are included on-chip, and are not required externally.

**Vg** – Negative gate voltage applied at a Vg pad is required to keep DC current consumption at a safely usable level. Negative gate bias must be applied *before* applying a positive drain voltage at the Vd pads. The 4 Vg pads are connected through large resistors on-chip, so gate bias can be to any – or multiple - Vg pads to apply gate bias. We recommend -0.6 V gate bias for efficient high-gain LO drive. A more negative gate bias will provide lower gain with lower power consumption, and a less negative gate bias will provide higher gain and marginally higher output power with higher power consumption.

**Vd**- Each Vd pad supplies the drain voltage to a different stage of this amplifier and can safely and functionally handle supply voltages between 2 and 4 Volts. Apply negative Vg *before* applying positive Vd.

**DC/RF Ground** – The back of the chip should be connected to a low noise RF and DC ground with very low electrical and thermal resistance for high frequency operation and thermal heat sinking.

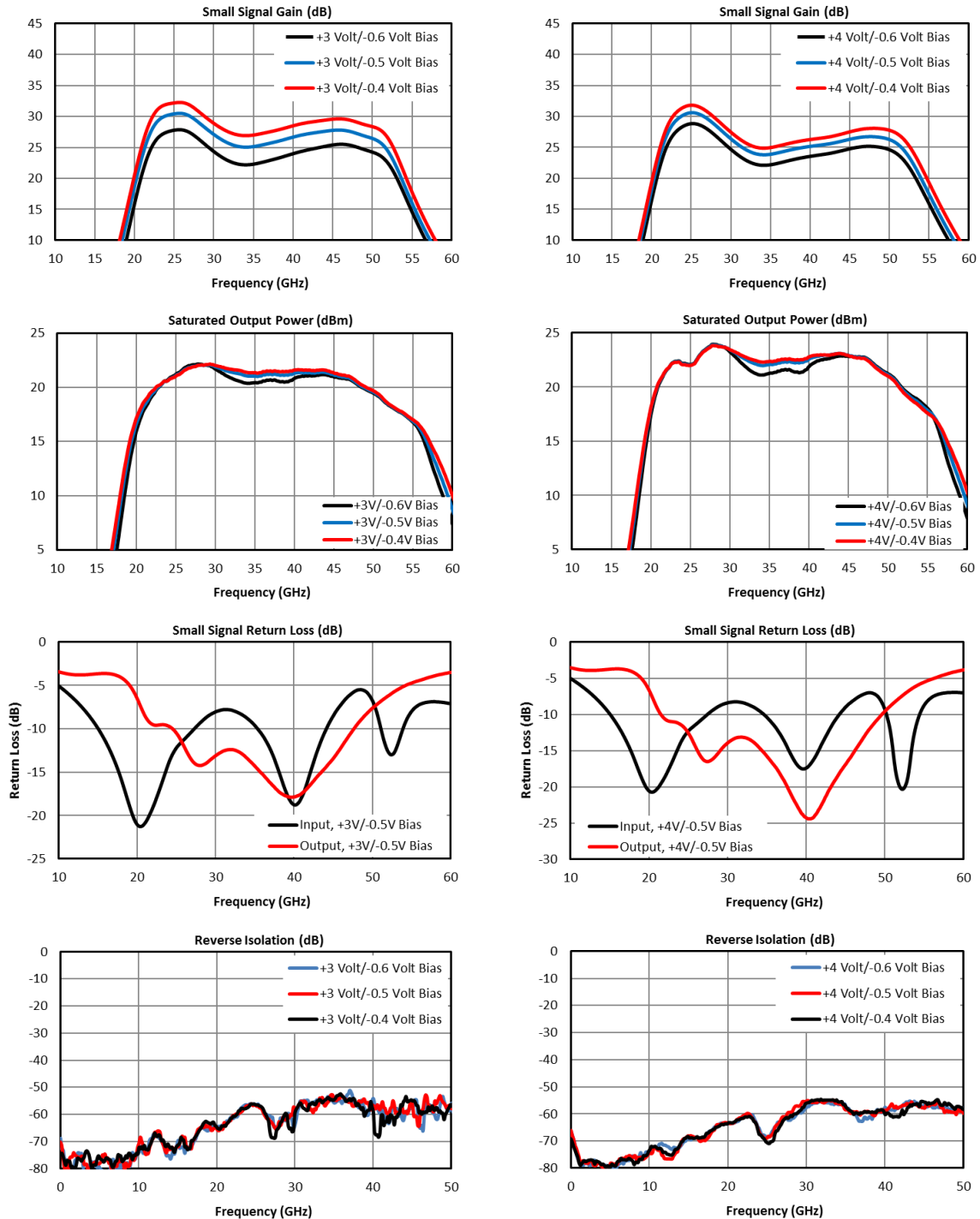
**BROADBAND AMPLIFIER**

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Frequency 20 to 55 GHz

On-chip Probe Data

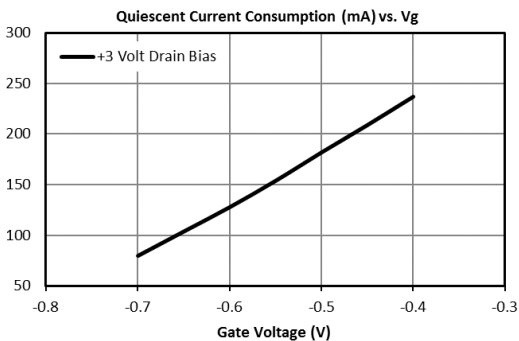
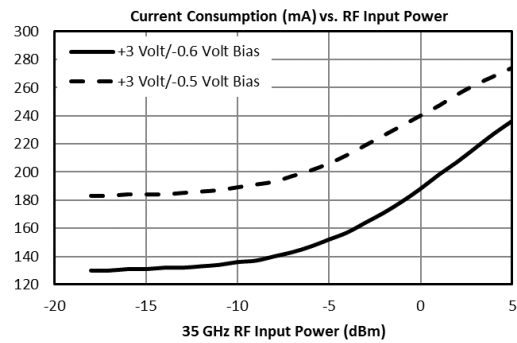
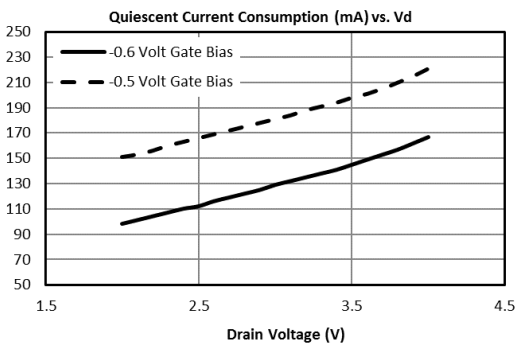
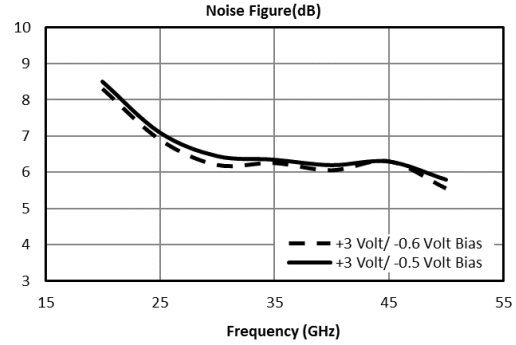
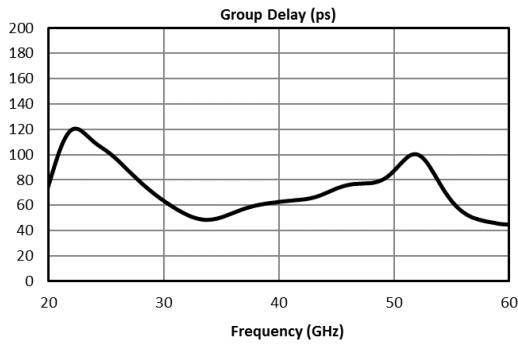
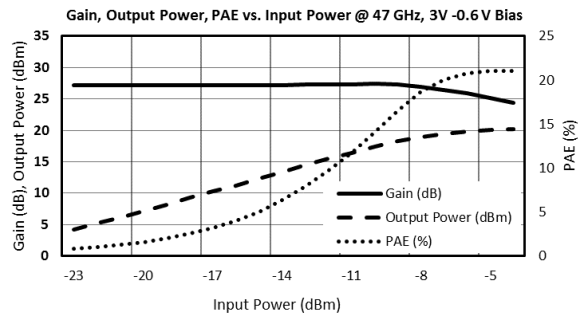
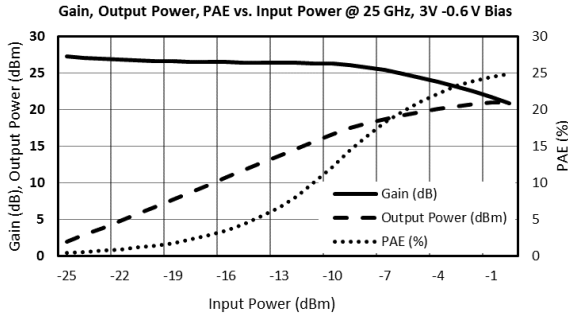


# BROADBAND AMPLIFIER

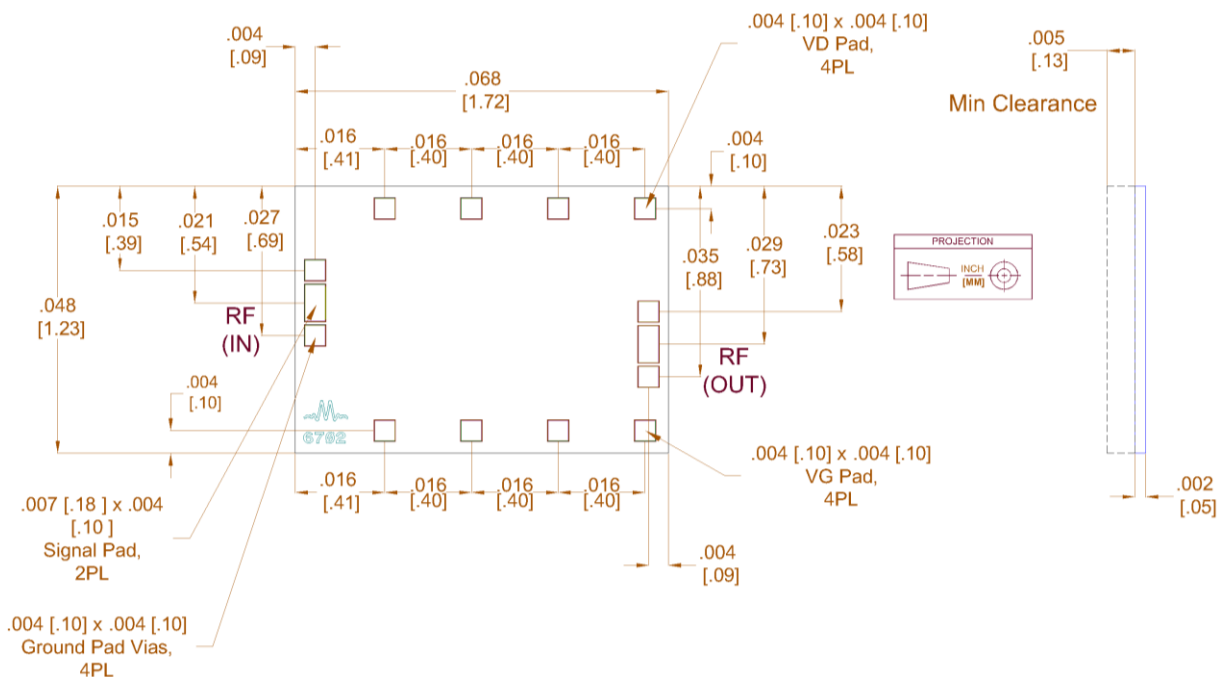
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# AMM-6702

Frequency 20 to 55 GHz



**Chip Outline Drawing**



1. RF GSG probe pitch is 150  $\mu$ m
2. CH substrate is .002 inches thick GaAs
3. I/O traces finish is 3.3 microns Au. Ground plane finish is 5 microns Au.
4. Die are not passivated.

**Handling Precautions**

**General Handling** Chips should be handled with care using tweezers with edge pick only. Users should take precautions to protect chips from direct human contact that can deposit contaminants, like perspiration and skin oils on any of the chip's surfaces. Chip surface has fragile and unprotected air bridges.

**Static Sensitivity** GaAs MMIC devices are sensitive to ESD and should be handled, assembled, tested, and transported only in static protected environments.

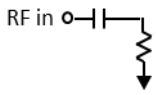
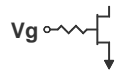
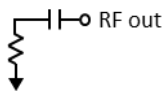
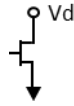

**Cleaning and Storage** Do not attempt to clean the chip with a liquid cleaning system or expose the bare chips to liquid. Once the ESD sensitive bags the chips are stored in are opened, chips should be stored in a dry nitrogen atmosphere.

# BROADBAND AMPLIFIER

# AMM-6702CH

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Frequency 20 to 55 GHz

Port Descriptions		
Function	Description	Interface Schematic
RF in	This pin is DC blocked and matched to 50 Ω.	
Vg1 - Vg4	Gate control for the amplifier. External decoupling capacitors are recommended. Gate pads are resistively connected on chip, and biasing a single pad will bias the other 3 gate bias ports. <i>Gate bias must be applied before drain bias is applied to prevent catastrophic damage to IC.</i>	
RF out	This pad is DC blocked and matched to 50 Ω.	
Vd1 - Vd4	Drain Bias ports must all be connected to a 2-4 volt power supply. Refer to functional diagram on page 2 of datasheet to see recommended external bypass circuitry to prevent low-frequency oscillations. <i>Gate bias must be applied before drain bias is applied to prevent catastrophic damage to IC.</i>	
GND	Back of chip should be connected to RF/DC ground with low electrical and thermal resistance.	

Absolute Maximum Ratings	
Parameter	Maximum Rating
Positive Bias Voltage	4.5 V
Positive Bias Current	400 mA
Negative Bias Voltage	-2 V
Negative Bias Current	2 mA
RF Input Power	+24 dBm
Power Dissipation	1.5 W
ESD (Human Body Model)	Class 0
Operating Temperature	TBD
Storage Temperature	TBD

DATA SHEET NOTES:

1. Specifications are subject to change without notice. Contact Marki Microwave for the most recent specifications and data sheets.

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