

## BROADBAND DISTRIBUTED AMPLIFIER

## ADM-5931CH

The ADM-5931CH is a broadband, power-efficient, GaAs PHEMT distributed amplifier chip. The ADM-5931CH is designed to provide optimal LO drive for T3 mixers. Typically, it provides 11 dB of gain and +18 dBm saturated output power while requiring only 85 mA of current. T3 linearity is enhanced by ADM-5931's extended high frequency gain and lower even harmonic generation when compared to other distributed amplifiers in our catalog. It can be biased with internal circuitry, or with an external bias network for lower voltage and single supply operation. Additional applications include amplification of clock signals and general-purpose driver requirements in electronic warfare and test and measurement.



Bare Die

### Features

- Low power consumption
- Optimized for use as a [T3 LO buffer amplifier](#)
- 2<sup>nd</sup> and 4<sup>th</sup> Harmonic Suppression
- 3<sup>rd</sup> and 5<sup>th</sup> Harmonic Generation
- Broadband 50  $\Omega$  Matching
- Unconditionally Stable

**Electrical Specifications** - Specifications measured in a 50-Ohm system.

| Parameter                                       | Frequency (GHz) | Typical |    |
|---|-----------------|---------|----|
| Input for Saturated Output (dBm)                | DC to 28        | +8      |    |
| Output 1 dB Compression (dBm)                   |                 | +16     |    |
| Saturated Output Power with negative bias (dBm) |                 | +18     |    |
| Small Signal Gain with negative bias (dB)       |                 | 11      |    |
| Input Return Loss (dB)                          |                 | 16      |    |
| Output Return Loss (dB)                         |                 | 14      |    |
| Noise Figure (dB)                               |                 | 6       |    |
| Third Order Output Intercept Point (dBm)        |                 | 27      |    |
| Phase Noise (10 kHz Offset) (dBc/Hz)            |                 | -153    |    |
| Bias Requirements, External (mA)                |                 |         |    |
| Vd: +5.0 to +7.0 / Vg: -0.25 Volts              |                 |         | 85 |
| Vd: +5.0 to +7.0 / Vg: 0 Volts                  |                 | 120     |    |

**Part Number Options**

| Model Number                                 | Description           | Green Status | Product Lifecycle | Export Classification |
|--|-----------------------|--------------|-------------------|-----------------------|
| ADM-5931CH                                   | Chip                  | RoHS         | Active            | EAR99                 |
| ADM-5931S                                    | Eval Board            |              |                   |                       |
| <a href="#">ADM-0012-5931SM</a> <sup>1</sup> | Surface Mount 3mm QFN |              |                   |                       |
| <a href="#">EVAL3-ADM-5931</a> <sup>1</sup>  | Eval Board            |              |                   |                       |
| <a href="#">ADM-0026-5931SM</a> <sup>1</sup> | Surface Mount 4mm QFN |              |                   |                       |
| <a href="#">EVAL4-ADM-5931</a> <sup>1</sup>  | Eval Board            |              |                   |                       |

<sup>1</sup>Note: Datasheets for other package options are available on the Marki Microwave website

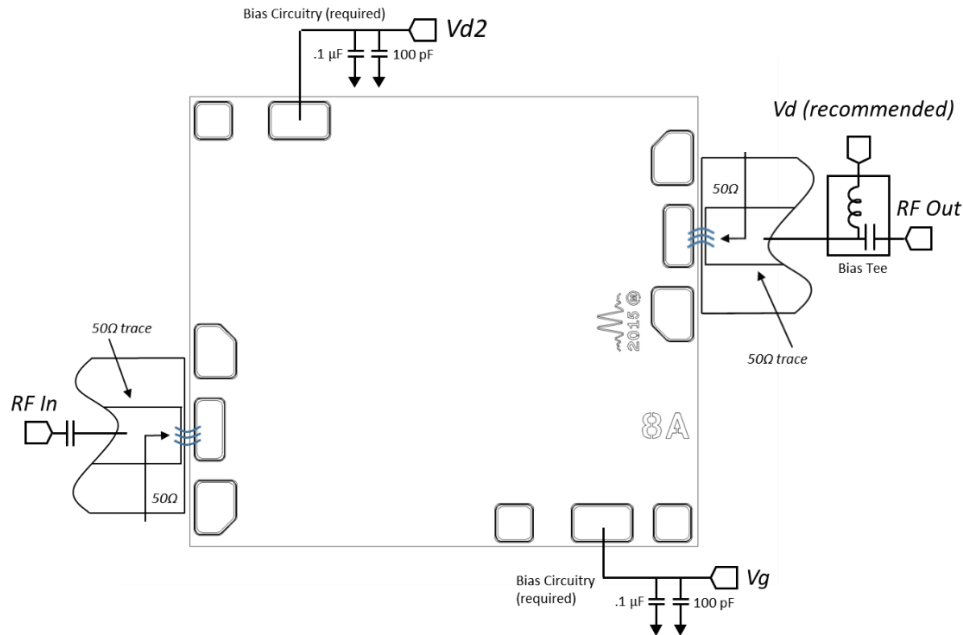
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Frequency DC to 28 GHz

Functional Diagram



## Biasing and Operation

**RF In / RF Out** – Input and output signals should be connected by 50 ohm microstrip or coplanar traces to well matched 50 ohm sources and loads. DC blocking capacitors and bias tees are required.

**Vg** – Negative gate voltage is optional to improve lifetime of the amplifier and reduce current consumption. Harmonic generation is also significantly affected by the negative gate voltage level. It may be supplied through the Vg pad or through the RF input pad using an external bias tee

**Vd**- It is recommended that bias voltage Vd is applied through a bias tee on the RF output, but bias supply can also be supplied to Vd through Vd2 pad if desired. This will result in increased operating temperature and slightly reduced gain and power output. Bias supply should be voltage limited below 9 V and current limited below 150 mA at all times. The operational bias voltage should be between 3 V and 7 V for full small-signal gain, or between 5 V and 7 V for full gain, linearity and power output. If bias tee on RF output is used, pad Vd2 voltage should be left unconnected (*not* grounded).

**Bias Circuitry** – The capacitors on the Vd and Vg lines prevent low frequency oscillation. They may be reduced or omitted in bias circuits with sufficient low-frequency loss. Designers are encouraged to experiment if they want to modify or omit the bias circuitry.

**DC/RF Ground** – The back of the chip should be connected to a low noise RF and DC ground with very low electrical and thermal resistance for high frequency operation and thermal heat sinking.

*Warning: GaAs MMIC devices are susceptible to Electrostatic Discharge. Use proper ESD precautions when handling these items.*

| Revision Code | Revision Date | Comment                   |
|---------------|---------------|---------------------------|
| -             | January 2018  | Datasheet Initial Release |

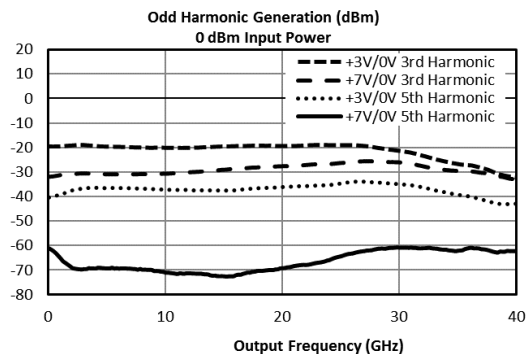
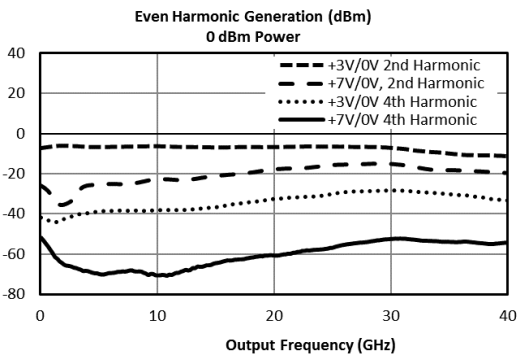
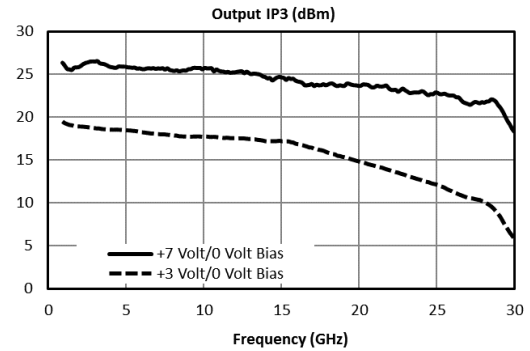
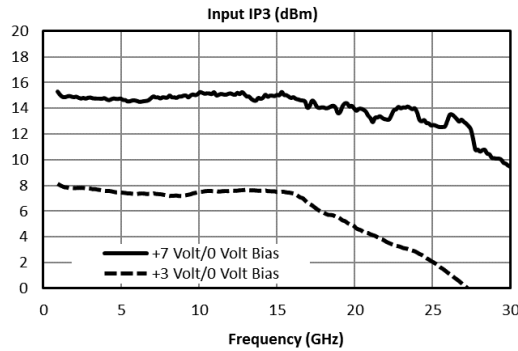
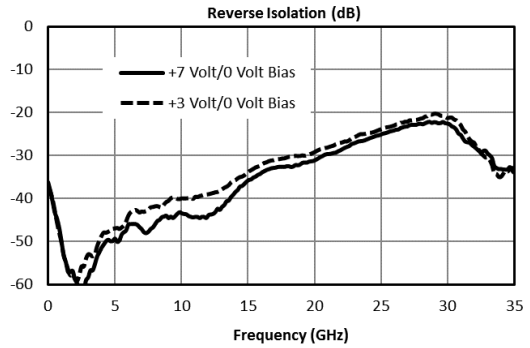
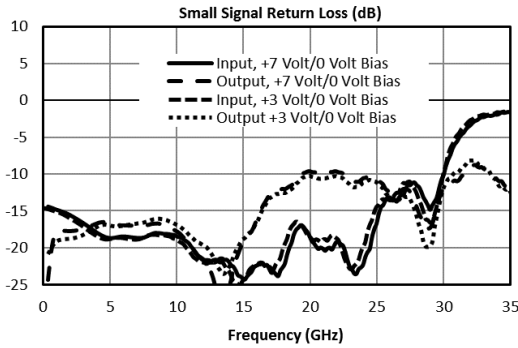
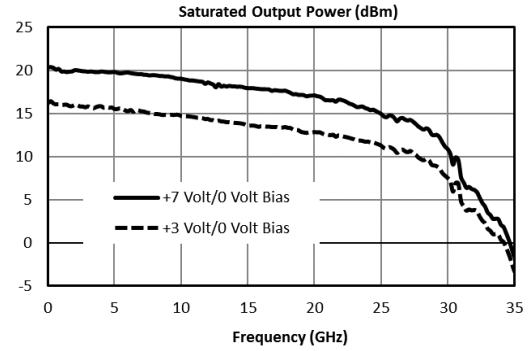
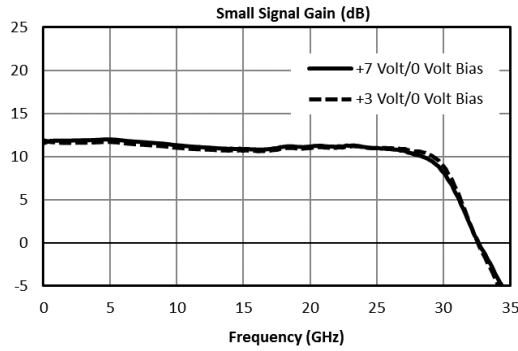
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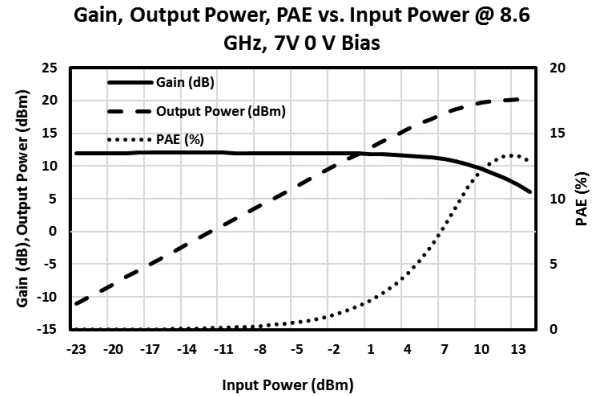
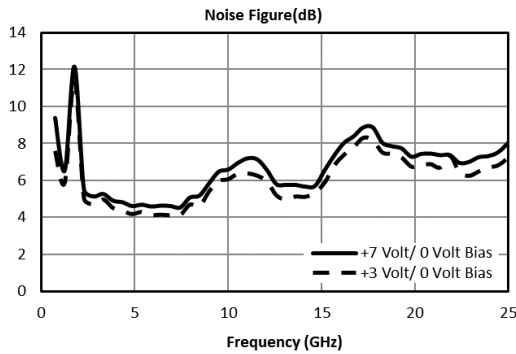
Typical Performance: Positive Only (+3, +7V) Bias (Bias tee on RF output), Grounded Gate (Bias tee on RF input)



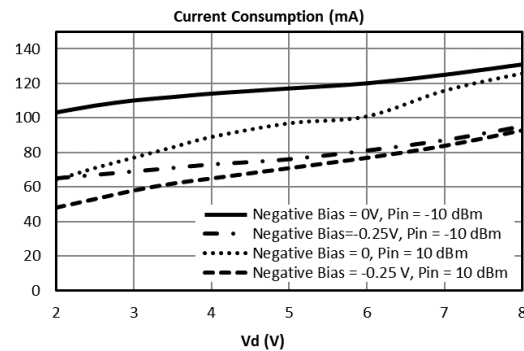
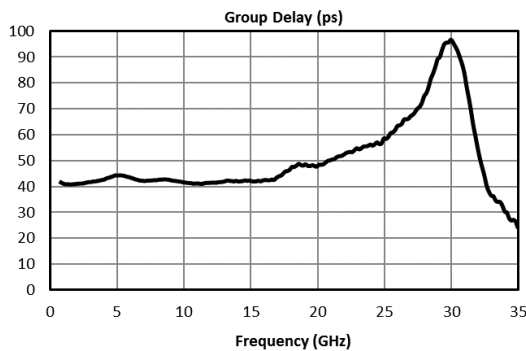
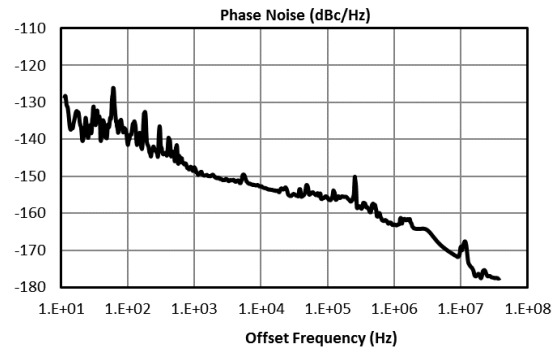
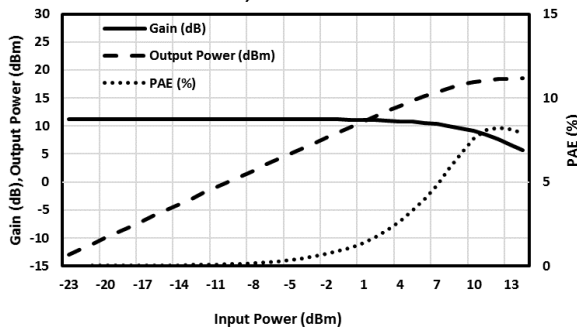
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Typical Performance: Positive Only (+3 to +7V) Bias, Grounded Gate (Continued)



Gain, Output Power, PAE vs. Input Power @ 17.25 GHz, 7V 0 V Bias



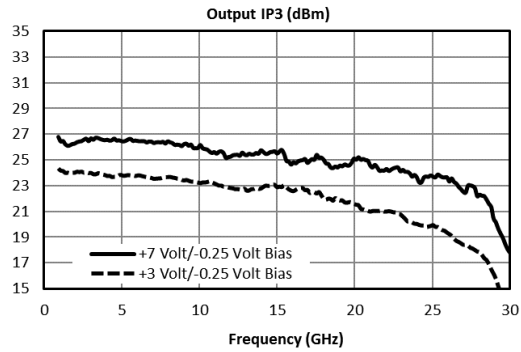
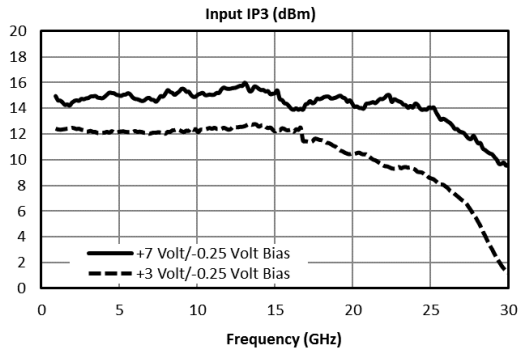
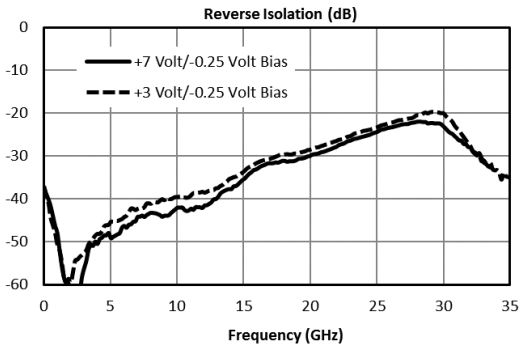
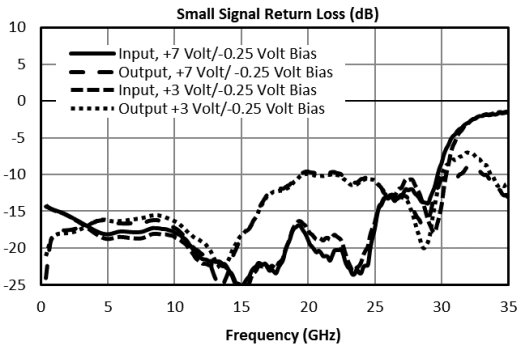
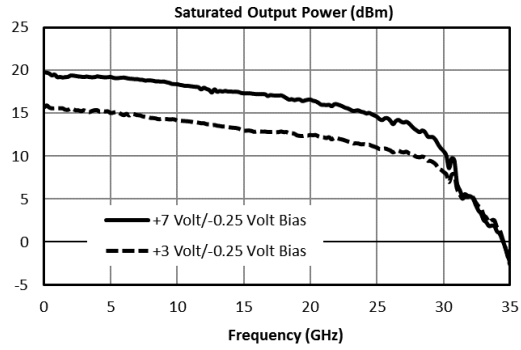
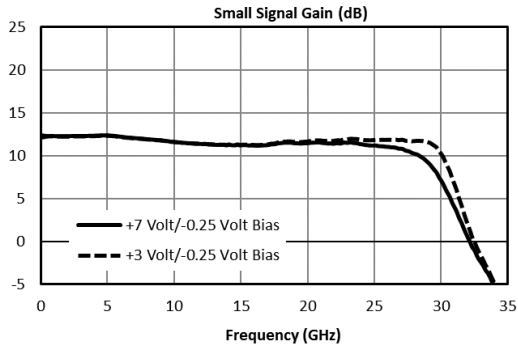
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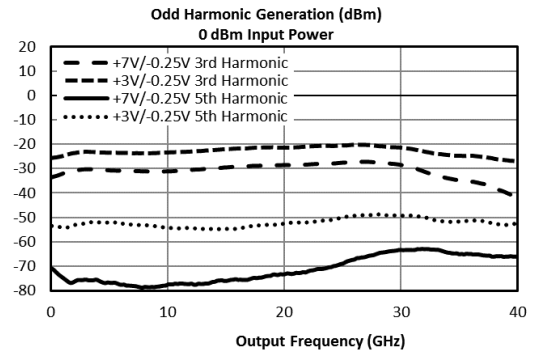
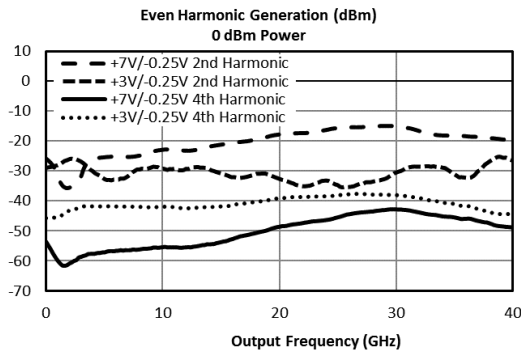
Typical Performance: Positive (+3, +7V) Bias, -0.25 V Negative Bias



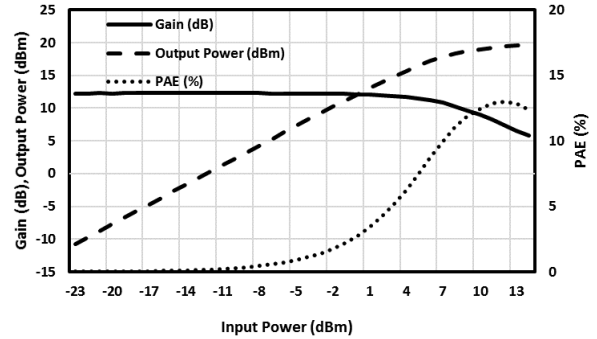
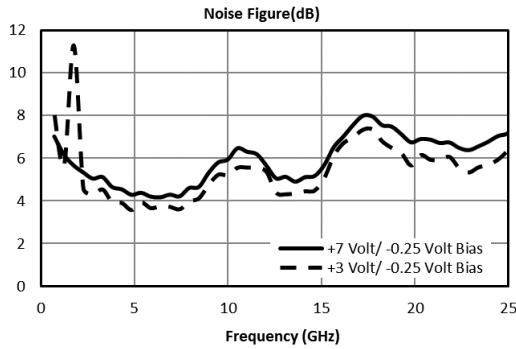
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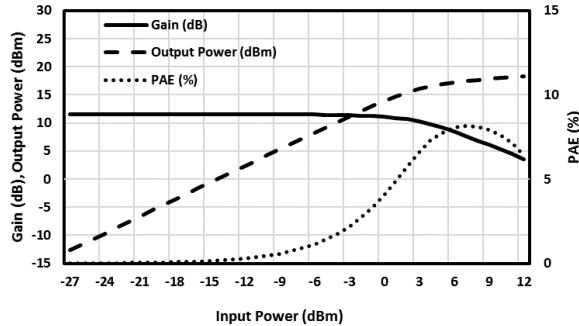
Typical Performance: Positive (+3, +7V) Bias, -0.25 V Negative Bias (Continued)



Gain, Output Power, PAE vs. Input Power @ 8.6 GHz, 7V -0.25 V Bias



Gain, Output Power, PAE vs. Input Power @ 17.25 GHz, 7V -0.25 V Bias



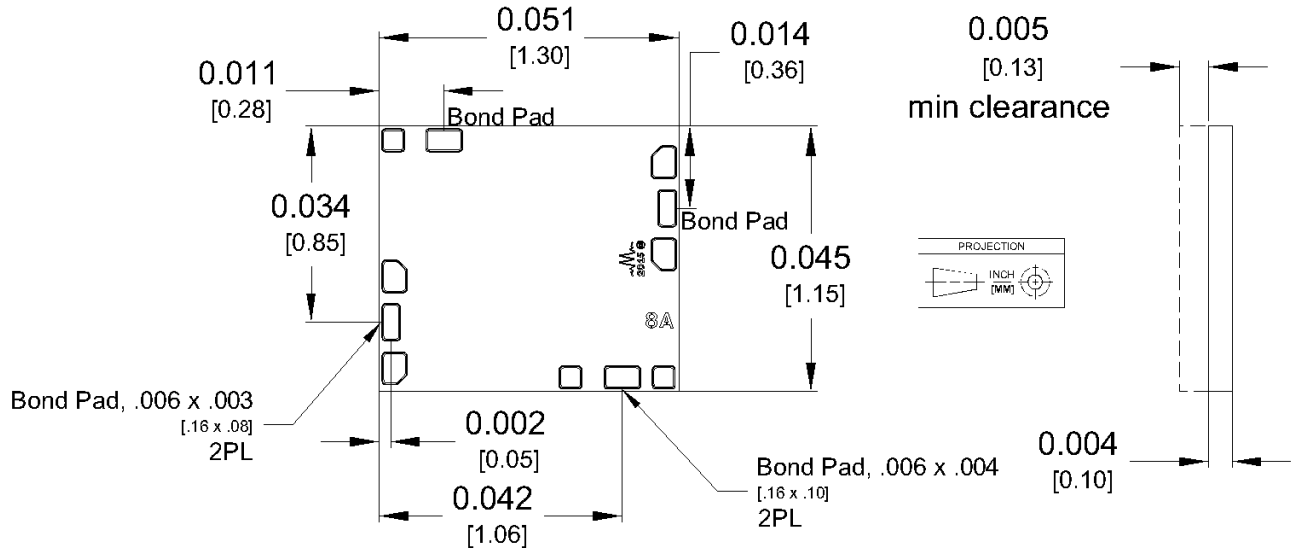
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Frequency DC to 28 GHz

Chip Outline Drawing


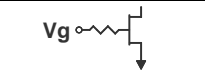

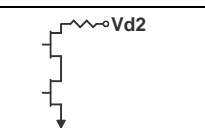



1. CH Substrate material is .004 thick GaAs.
2. I/O traces and ground plane finish are 2 microns Au
3. RF GSG probe pitch is 200 μm
4. All unlabeled pads are ground pads



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# ADM-5931CH

| Port Descriptions |  |   |
|-------------------|--|---|
| Function          | Description  | Interface Schematic   |
| RF in             | This pin is DC coupled and matched to 50 $\Omega$ .  |  |
| Vg                | Gate control for the amplifier. External decoupling capacitors are required.                 |  |
| RF out / Vd       | This pad is DC coupled and matched to 50 $\Omega$ .  |  |
| Vd2               | Optional drain bias port. External decoupling capacitors are required.                       |  |
| GND               | Back of chip should be connected to RF/DC ground with low electrical and thermal resistance. |  |

| Absolute Maximum Ratings          |                 |
|-----------------------------------|-----------------|
| Parameter                         | Maximum Rating  |
| Positive Bias Voltage             | 9 V             |
| Positive Bias Current             | 150 mA          |
| Negative Bias Voltage             | -0.3 V          |
| Negative Bias Current             | 2 mA            |
| RF Input Power                    | +20 dBm         |
| Power Dissipation                 | 2 W             |
| Thermal Resistance, $\theta_{jc}$ | 0.873 C/W       |
| ESD (Human Body Model)            | Class 0         |
| Operating Temperature             | -55°C to +85°C  |
| Storage Temperature               | -65°C to +150°C |

DATA SHEET NOTES:

1. Specifications are subject to change without notice. Contact Marki Microwave for the most recent specifications and data sheets.

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