

## BROADBAND DISTRIBUTED AMPLIFIER

## ADM-0126MSM

The ADM-0126MSM is a broadband, efficient GaAs PHEMT distributed amplifier with an integrated bias tee in a 4mm QFN surface mount package. It offers 11 dB typical gain and 17 dBm typical output power at 1 dB compression for only 75 mA of current. It is operated with a 5-7 volt positive bias and an optional current reducing negative voltage. Applications include amplification of LO drive signals for 'L', 'M', and 'I' level mixers, clock signals, and other general purpose driver applications in electronic warfare and test and measurement. It is an excellent alternative to competing GaAs PHEMT distributed amplifiers.



### Features

- Optimized for use as a [T3 LO buffer amplifier](#)
- Suitable for driving M and L level diode mixers with +5V bias
- Suitable for driving I diode mixers with +8V bias
- Optional Positive Bias Operation
- Integrated Blocking Capacitors and Inductors
- +17 dBm Typical Saturated Output Power
- Buffer- Amplifiers for Mixer LO
- 3<sup>rd</sup> and 5<sup>th</sup> Harmonic Generation
- Broadband 50  $\Omega$  Matching
- Unconditionally Stable

**Electrical Specifications** - Specifications guaranteed from -55 to +85°C, measured in a 50-Ohm system.

Parameter	Frequency (GHz)	Min	Typ	Max	
Input for Saturated Output (dBm)	1-26.5	+5	+10	+12	
Output 1 dB Compression (dBm)			+15		
Saturated Output Power with negative bias (dBm)				+17	
Small Signal Gain with negative bias (dB)				11	
Return Loss (dB)				10	
Noise Figure (dB)				4	
Third Order Output Intercept Point (dBm)				25	
Bias Requirements (mA)				75	
Vd: +5.0 to +7.0 / Vg: -0.20 Volts Vd: +5.0 to +7.0 / Vg: 0 Volts				90	

***GaAs MMIC devices are susceptible to Electrostatic Discharge. Use proper ESD precautions when handling these items.***

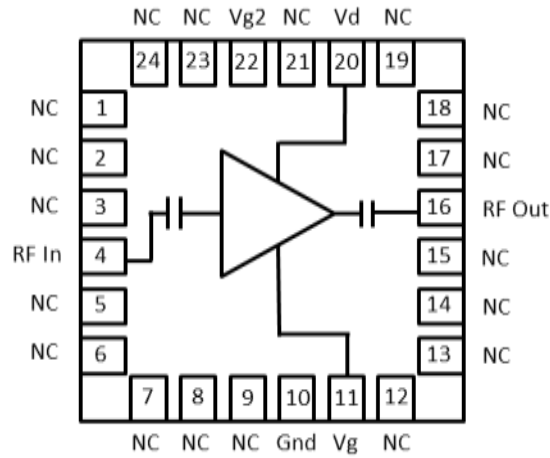
# BROADBAND DISTRIBUTED AMPLIFIER

# ADM-0126MSM

Page 2

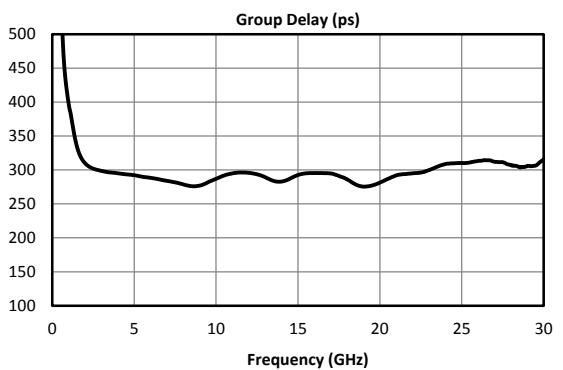
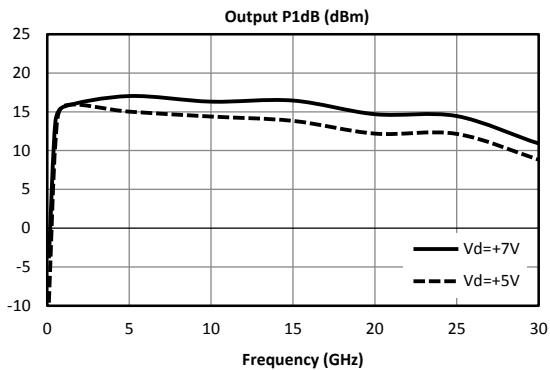
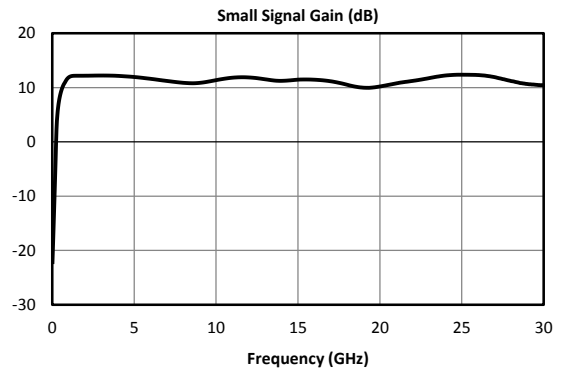
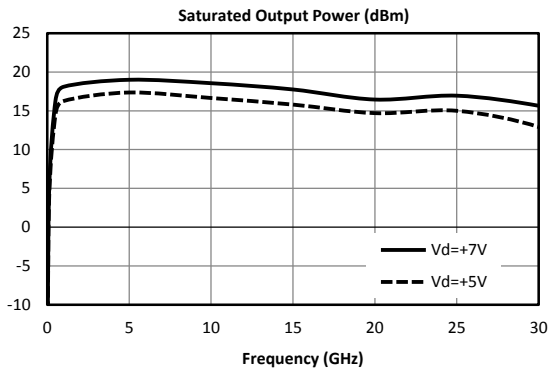
Frequency 1 to 26.5 GHz

Functional Diagram



Typical Performance

(Performed at +5/-0.2V and 27°C unless otherwise indicated)



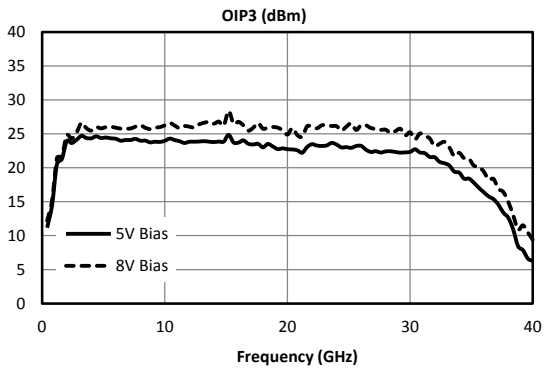
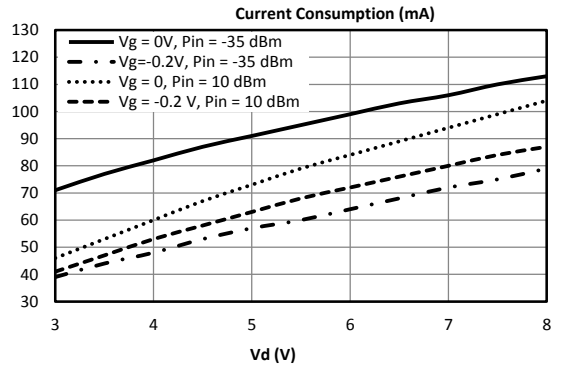
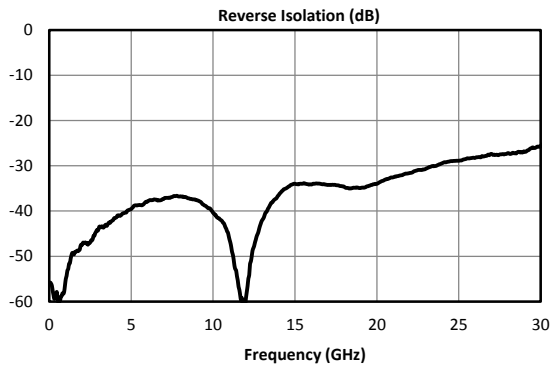
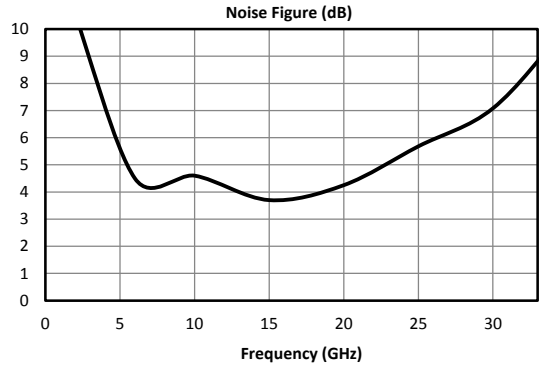
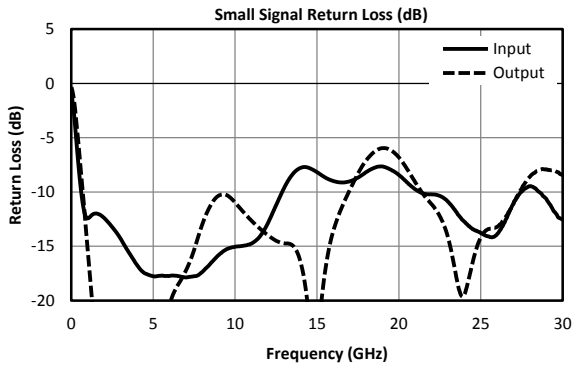


# BROADBAND DISTRIBUTED AMPLIFIER

# ADM-0126MSM

Page 3

Frequency 1 to 26.5 GHz



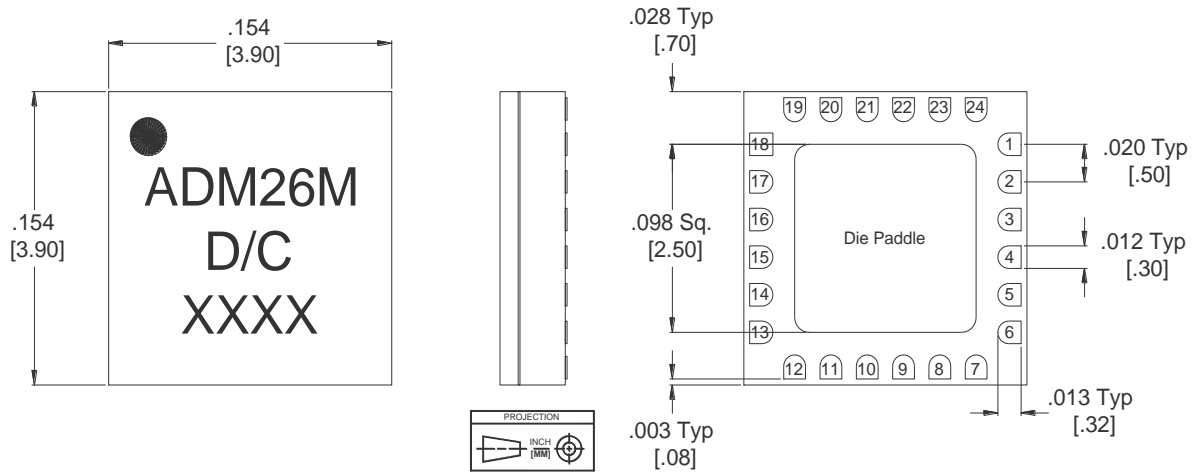
# BROADBAND DISTRIBUTED AMPLIFIER

# ADM-0126MSM

Page 4

Frequency 1 to 26.5 GHz

## Outline Drawing

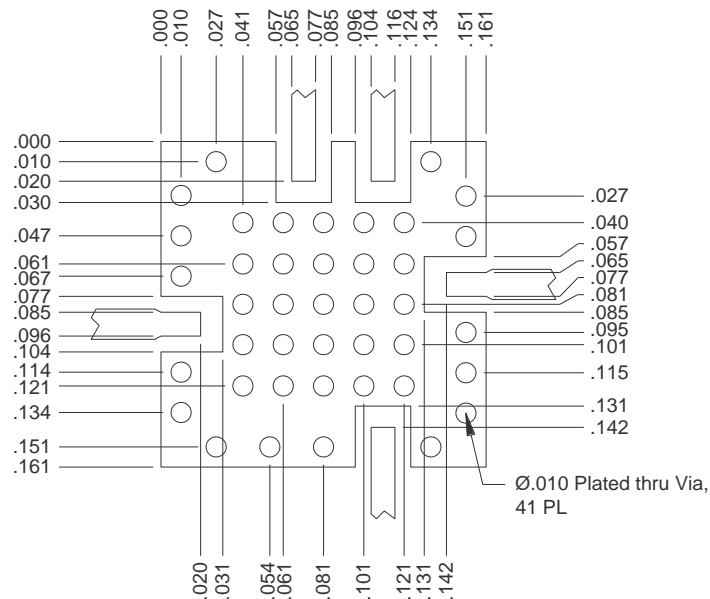


Substrate material is Ceramic.

I/O Leads and Ground Paddle are 1.4±0.6 microns Au over 1.3 microns Ni.

All unconnected pads should be connected to PCB RF ground.

## PCB Footprint Drawing



## QFN-Package Surface-Mount Landing Pattern

[Click here for a DXF of the above layout.](#)

[Click here for leaded solder reflow.](#) [Click here for lead-free solder reflow.](#)



# BROADBAND DISTRIBUTED AMPLIFIER

# ADM-0126MSM

Page 5

Frequency 1 to 26.5 GHz

Pin Descriptions			
Pin Number	Function	Description	Interface Schematic
1-3,5-9,12-15,17-19,21,23,24	NC	These pins are not connected internally. Datasheet performance is tested with NC pins grounded.	
4	RF in	This pin is AC coupled and matched to 50 $\Omega$ .	
11	Vg	Gate control for the amplifier. Adjust to achieve $I_{dd} = 85$ mA (should be near -0.2V). External bypass capacitors and Q reduction resistor are recommended.	
16	RF out	This pad is AC coupled and matched to 50 $\Omega$ .	
20	Vd	Power supply voltage for the amplifier. External bypass capacitors are required.	
22	Vg2	Optional gate control if AGC is required. Leave Vg2 open circuited if AGC is not required. Typical $V_{g2} = -2$ V to 2.4V	
10, Paddle	GND	Ground pad should be connected to RF/DC ground with low electrical and thermal resistance.	

Absolute Maximum Ratings	
Parameter	Maximum Rating
Positive Bias Voltage	9 V
Positive Bias Current	200 mA
Negative Bias Voltage	-2 V
Negative Bias Current	2 mA
RF Input Power	+15 dBm
Power Dissipation	875 mW
ESD (Human Body Model)	Class 0
Operating Temperature	-55°C to +85°C
Storage Temperature	-65°C to +150°C

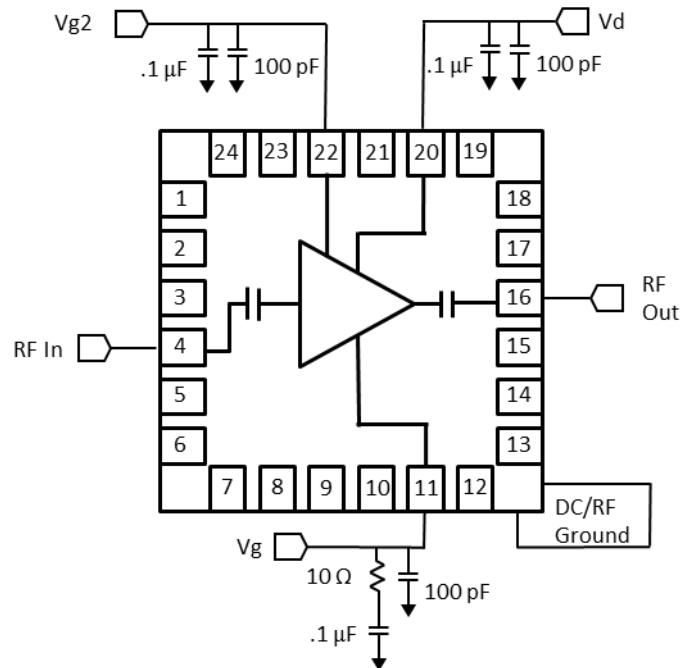
## BROADBAND DISTRIBUTED AMPLIFIER

ADM-0126MSM

Page 6

Frequency 1 to 26.5 GHz

Application Circuit



### Biasing and Operation

**RF In / RF Out** – Input and output signals should be connected by 50 ohm microstrip or coplanar traces to well matched 50 ohm sources and loads. No external bias capacitor or inductor is required.

**Vg /Vg2** – Bias on these pins is optional. Biasing of -0.2 V on Vg can reduce the current draw from Vd by 35 mA (from 120 mA to 85 mA) and power consumption by 280 mW (from 960 mW to 680 mW). As with Vd, it is recommended that the user supply a broadband, low impedance signal path to ground on this pin by providing multiple capacitance values with different resonant points to ground. It is also recommended to supply a 10 Ω resistor in series with any bypass capacitor with a value above 1 nF for Vg to eliminate self-resonant points in the circuit.

**Vd**- Bias supply on Vd should be voltage limited below 9 V and current limited below 200 mA at all times. The operational bias voltage should be between 5 V and 8 V for full gain, efficiency, and linearity. In general gain, linearity, and output power will increase marginally with increased voltage from 5 to 8 V. As with Vg/Vg2, it is recommended that the user supply a broadband, low impedance signal path to ground on this pin by providing multiple capacitance values with different resonant points to ground.

**DC/RF Ground** – The ground paddle of the QFN should be connected to a low noise RF and DC ground with very low electrical and thermal resistance for high frequency operation and thermal heat sinking.

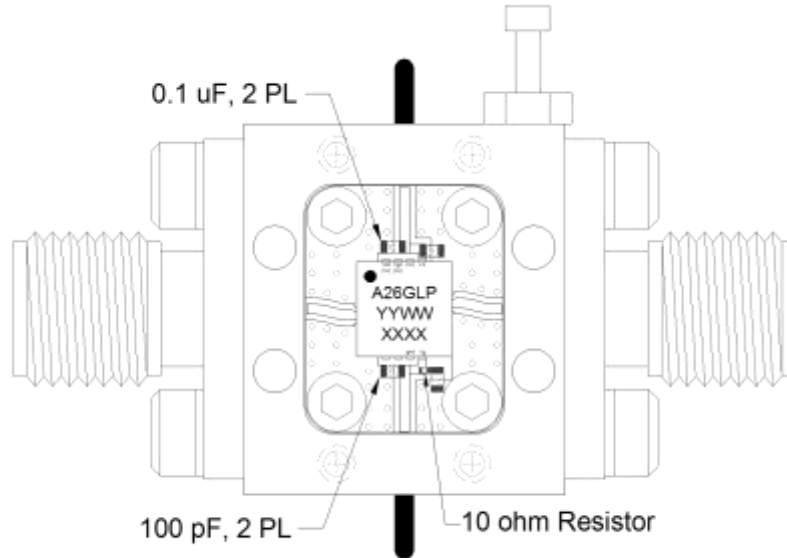
# BROADBAND DISTRIBUTED AMPLIFIER

# ADM-0126MSM

Page 7

Frequency 1 to 26.5 GHz

Evaluation Board



The evaluation module follows Marki standard assembly and evaluation procedures to give optimal performance for datasheet characterization. Actual performance will depend on substrate material, bypass capacitors, resistors, connectors, quality of bias current/voltage source, and assembly process.

Evaluation Board Bill of Materials	
Item	Description/Part Number
Connectors	Southwest 214-510SF
Bias Pins	Kovar
Housing	Aluminum
Circuit	8 mil Rogers 4003
0.1 uF Capacitor	AVX 0402YD104KAT2A
10 Ω Resistor	Venkel CR0201-20W-100JT
100 pF Capacitor	KEMET C0402C101K4GACTU
A26LGP	ADM-0126MSM

DATA SHEET NOTES:

1. Specifications are subject to change without notice. Contact Marki Microwave for the most recent specifications and data sheets.

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